Wideband Variable Gain Amplifier for D-band Backhaul Transceiver in 55nm BiCMOS Technology

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***Abstract*— This paper presents a Variable Gain Amplifier (VGA) for D-band (130-175) GHz backhaul transceiver using 55nm BiCMOS Technology. It includes a linear-in-dB control circuit to achieve a dB-linear gain that can be steered by a single analog voltage. A 6 dB gain with a control range of over 20 dB, and an input power at -1dB compression better than -10 dBm have been achieved over the full D-band and gain range. The input and output return loss are both greater than 7 dB. This circuit has been designed to be a building block in our future transmitter and receiver chips for a phased array antenna in D-band.**

***Keywords*— Backhaul, millimeter-wave, D-Band, BiCMOS, Wideband Amplifier, Variable Gain Distributed Amplifier (VGDA).**

I. Introduction

DATA transmission in D-band with beam steering capability [1] can achieve data rates of 100 Gb/s with a reconfigurable meshed backhaul network to adjust the network capability to the user requirements.

However, millimeter-wave active antennas require a high degree of integration since the distance between the elements decreases with frequency [2]. At the same time, it is necessary to have broadband circuits to cover the full D-band (30%), and design linear circuits to increase the modulation order and achieve the highest throughput.

GaAs and InP technologies are traditionally used to design wideband circuits at millimeter-waves because the maximum oscillation frequency and breakdown voltages are higher [3] compared to other technologies. However, they do not allow the integration of complex chips, including digital [4], analog and millimeter-wave circuits provided by silicon technologies. Therefore, the 55nm BiCMOS technology from STMicroelectronics [5] has been selected because it provides both bipolar transistors with a maximum oscillation frequency (fmax) above 350 GHz and the integration capabilities of 55nm CMOS technology.

If various broadband amplifiers are required in the transmitter and the receiver, the VGA is a key function to consider both on receive and transmit because it allows to maximize the dynamic range of the overall system by controlling the transmitted signal power or adjusting the received signal amplitude to maintain signal quality and overcome gain variations in the transceiver chains.

This paper presents the design of the VGA as a demonstration of 55-nm BiCMOS technology to develop wideband circuits for future phased array in D-band. Section II describes the architecture, design, and implementation of the VGA. Section III shows the linear and non-linear characterization results. Finally, section IV concludes the article.

II. Circuit design & Implementation

A. VGA Circuit Design

Designing a broadband VGA with wide gain control range and enough linearity to ensure the highest modulation scheme, is always a challenge. Especially when the maximum frequency ratio of the components to the working frequency is around 2. In this context, the VGA will be based on a distributed architecture that can achieve a bandwidth of several octaves in conjunction with good matching and gain flatness, both on SiGe [6] and InP [7] technologies. However, these advantages induce a significant trade-off as the distributed amplifiers require more DC power compared to tuned amplifiers.

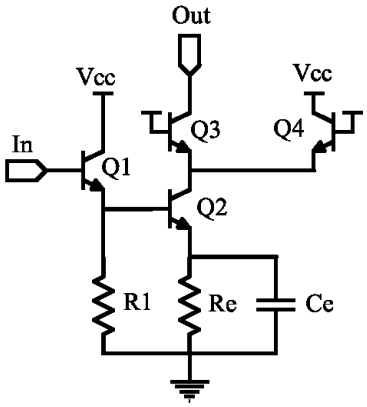
The Variable Gain Distributed Amplifier (VGDA) consists of three identical unit gain cells separated by microstrip transmission lines to obtain a good compromise between bandwidth, gain, chip area, and power consumption.

The schematic of the unit gain cell is shown in Fig. 1 and contains an emitter follower (Q1) with resistor current source (R1) and a cascode stage (Q2 & Q3) with parallel R-C circuit in the emitter. The base node of the common-base device of the cascode structure was carefully studied and simulated because it can cause the real part of the output impedance to become negative, which can lead to instabilities. In our application, the purpose of this R-C circuit is to both adjust the gain-frequency slope and the low frequency cut-off to have no out-of-band gain

This work has received funding from the European Union's H2020 research and innovation program under grant agreement No 761390, acronym: DREAM.

and therefore reduce the level of any out-of-band interferer, spurious or sub-harmonics of the Local Oscillator (LO).

Fig. 1. Simplify schematic of the unit gain cell with current steering



The method of current steering has been selected to implement the gain control function, and is well adapted from the cascode topology. The common-base transistor, Q3, is paired with a current transistor, Q4. By varying the transconductance of the common-base transistor through current steering, the gain of the cascode can be controlled by applying a differential voltage between the base of Q3 and Q4. A differential voltage is applied on the base of Q3 and Q4 using a linear control circuit in dB to achieve linear gain control of 20 dB when the voltage varies from 0 to 3.3 V. A series peaking line at the output of each cell is added to extend the bandwidth and meet specifications.

B. Implementation

A chip microphotograph of our VGDA is shown in Fig. 2. The microstrip transmission lines are composed of a thick top layer as a signal conductor, and a ground conductor that can be one or several interconnect layers connected together. It depends on the design and layout constraints.

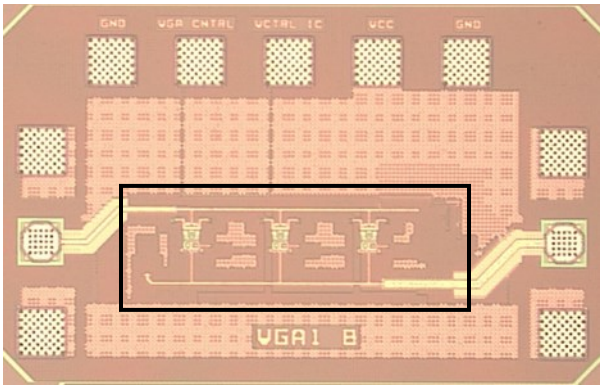


Fig. 2. Microphotograph of SiGe VGDA. The RF input is on the left, output on the right. Biasing is done through on-chip bias network. Overall chip size is 0.82 x 0.5 mm², but the core size (black contour rectangle is 0.4 x 0.14=0.056 mm²).

III. Simulation and Measurement Results

To fully characterize the VGA in D-band, two test benches have been setup to measure on wafer the linear and non-linear characteristics of the D-band amplifiers.

The S-parameter measurements were performed using a Keysight Technologies N5245A in addition with a Virginia Diode Inc. (VDI) millimeter-wave head VNAX DS and Cascade infinity waveguide probes. The calibration was done using on-wafer SOLT procedure and an Impedance Standard Substrate for 110 GHz and above from Cascade.

The input source of the scalar test bench is composed of a signal synthesizer followed by a VDI D-band frequency range extender and a mechanical attenuator to control the input level. The output power is measured with a VDI Erickson PM5 Calorimeter. The measurement system allows us a characterization from 110 GHz to 171 GHz. All losses of the measurement system are calibrated out. The estimated accuracy of the output power and gain are respectively 1 dB and 2 dB.

The S-parameter measurement results at maximum gain and nominal biasing settings are shown in Fig. 4. The measured and simulated results are very close, which validates the design procedure using:

1. The EM simulator to simulate all passive networks including the transition between the RF probe pads and the core circuit.
2. The ST design kit and the parasitic element extraction tool.

The VGA achieves a gain of around 6 dB with an upper 3 dB frequency of 160 GHz. The gain response is extremely flat and exhibits no peaking. The input and output return losses are respectively better than 8 dB and 10 dB over the full D-band.

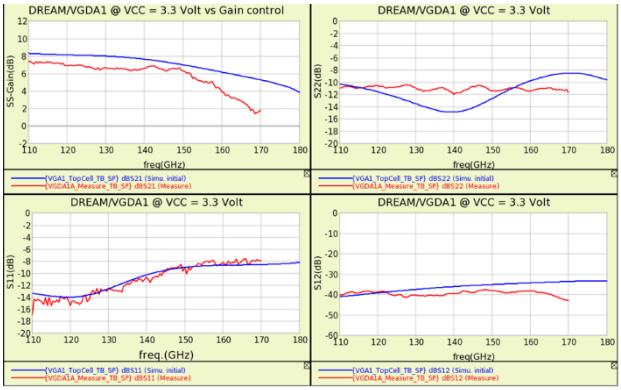


Fig. 4. S-parameter measurements in red and the simulations in blue at the maximum gain. All voltage supplies are 3.3 Volt (52 mA).

Figure 5 illustrates the capability of the VGDA to achieve 20 dB gain control and maintain the same gain flatness and bandwidth over all measured gain states. The group delay is around 12 ps, and the input and output return loss are both higher than 7 dB over D-band and all measured gain states.

The gain control (Fig. 6) is shaped with a flat response from 0 to at least 0.3 V to ensure that we can achieve maximum gain. Then, the gain decreases slowly with a slope around 6.0 dB/V. Over the D-band, the gain variation is better than 1dB.

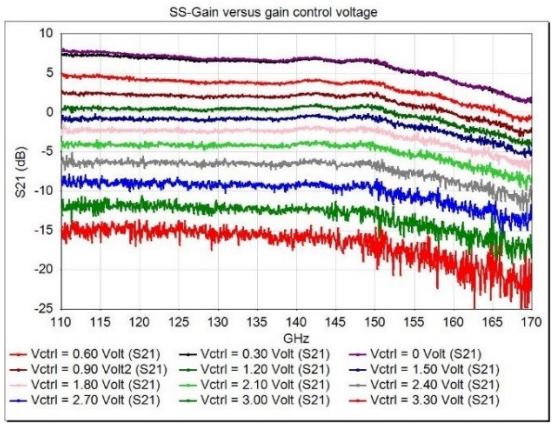


Fig. 5. SS-gain measurements versus gain control voltage (from 0 to 3.0 V in 0.3 V steps).

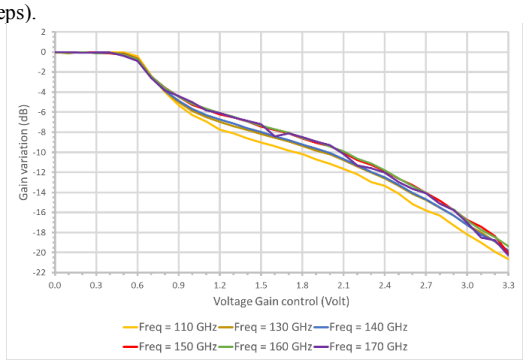


Fig. 6. Gain variation of the VGA at different frequency versus gain control voltage.

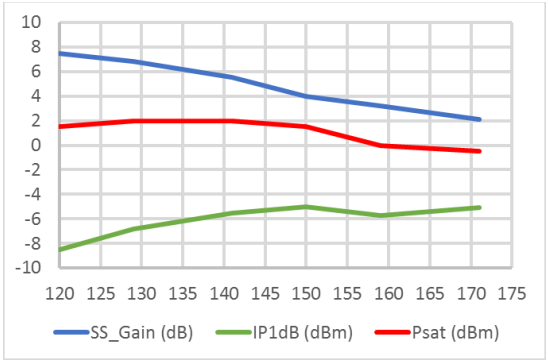


Fig. 7. Non-linear measurement results of VGA at the maximum gain.

I. SPECIFICATIONS VS. MEASUREMENTS

	Specification	Measurement
Operating frequency	130-175 GHz	120-170 GHz
Bandwidth	30%	35%
Gain range	> 20 dB	20 dB
Max. Gain	≈ 6 dB	≈ 6 dB
Gain ripple*	± 0.5 dB	± 0.2 dB
IP1dB	> -6 dBm	> -8 dBm**
Input return loss	> 10 dB	> 7 dB
Output return loss	> 10 dB	> 10 dB

(*) over 2 GHz bandwidth. (**) at maximum gain.

The input powers at 1dB compression (IP1dB) and saturated output power (Psat) are greater than -8 dBm and 0 dBm over the full D-band as shown in Fig. 7. The Power consumption of the VGDA is 171.6 mW. Based on our current data, the VGDA is still linear at 150 GHz for an input power of -10 dBm over the full gain control range which will guarantee that the signal quality is not affected by the gain reduction. However, an additional measurement is required to get an accurate value of IP1dB.

The measurements at D-band are in line with specifications and allow continued development of a wideband solution in D-band systems on a technology suitable for large integration and future phased array development.

IV. CONCLUSION

We presented a BiCMOS variable gain distributed amplifier as an interesting solution to cover our VGA requirements for future D-band communication systems. When compared to the current literature on millimeter-wave variable gain amplifiers [8-11], the VGA shows good performances in terms of bandwidth, gain flatness and linearity over wide gain control range, furthermore the compactness of the chip core size is only 0.056 mm².

The good agreement between simulations and measurements will help us in next development iteration, thus enabling their integration in future D-band backhaul transceivers.

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