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Deliverable D2.6:
Final report on D-band frequncy synthesis design

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Summary

This report presents measurement results of the D-band frequency multipliers for the LO chain that will be used to drive the I/Q modulators/demodulators in the transmitter and receiver. The LO chain upconverts a reference LO at X-band (12.5GHz) to D-band (150GHz). The multiplication factor of 12 is realized in steps of 3, 2, and 2. The first tripler and doubler, making a sextupler, are inside a separate chip. The last doubler has been fabricated as a sepratae chip for testing, but it will be integrated inside the up/down converters.
Performances of both chips have been characterized and show promising results to be used in the full demonstrator.

Confidentiality	Public

Contents

List of abbreviations

LO	Local oscillator
PN	Phase noise
Q factor	Quality factor
FMX6	Frequency multiplier by 6
FMX2	Frequency multiplier by 2
DP	Differential pair
TC	Trans-characteristic
GSG	ground-signal-ground
SPI	Serial-parallel interface
PDK	Process design kit
GSG	ground-signal-ground

List of symbols

Pin	Input power
Pout	Output power

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1. Introduction

Based on the specifications outlined in WP1, an LO chain has been designed to provide an LO signal at D-band. The LO chain is composed of a reference source at X-band followed by a frequency multiplier by 12 which multplies the frequency in steps of 3, 2, and 2. The first tripler and doubler were fabricated in the first tape-out of the project and presented in the deliverable D2.5. The tripler circuit successfully covered the required specifications, but the doubler needed refinements. Both circuits were redesigned and integrated into one frequency sextupler chip (FMX6) and sent to fabrication in the third tape-out of the project. Measurement results of this final FMX6 chip is presented in this deliverable.
Moreover, the last multiplication stage, FMX2, was fabricated in the second tape-out of the project. Measurement results of this chip is also covered in this deliverable.

2. Frequency synthesis chain

The overall architecture of the LO chain is shown in Figure 2.1. The proposed architecture allows to generate a precise and accurately tuneable oscillation at X-band using commercial frequency synthesis methods such as PLLs, and then up-convert it to D-band. Output of the X-band LO, single ended, is fed to the designed FMX6 chip. Output of this chip, at E-band, has a centre frequency of 75GHz. This output is in turn fed to the up/down converters whose first block is the D-band frequency doubler which in turn up-converts the local oscillation frequency to nominally 150GHz.

The frequency synthesis architecture, split in three different blocks, is conceived to meet system level specifications while minimizing risks, and to increase testing and debug flexibility. The X-band signal source is a commercial block that provides a clean (low phase noise and spurs) instrument-like synthesized signal. The FMX6 multiplier, with output in E-band (75GHz centre frequency) is implemented as a separate chip allowing to simplify test of the D-band up-/dn- converters by using an E-band laboratory signal source. The connection between FMX6 and FMX2 is done single ended to ease measurements of both chips and make easier the design of the PCB traces between the two chips carrying an E-band signal.

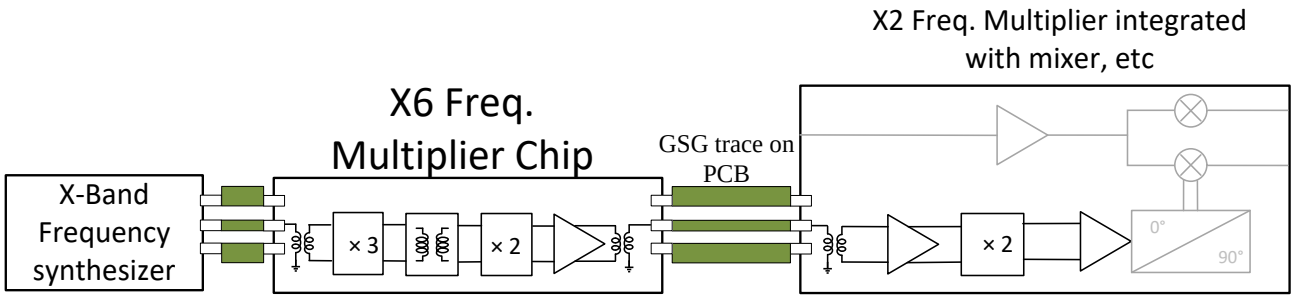

Figure 2.1. Full LO chain

3. The E-band multiplier by 6

3.1 Chip architecture

Figure 3.1 shows the overall architecture of the FMX6 chip, fully designed and fabricated in STMicroelectronics BiCMOS55nm technology. It converts the input X-band signal to E-band.

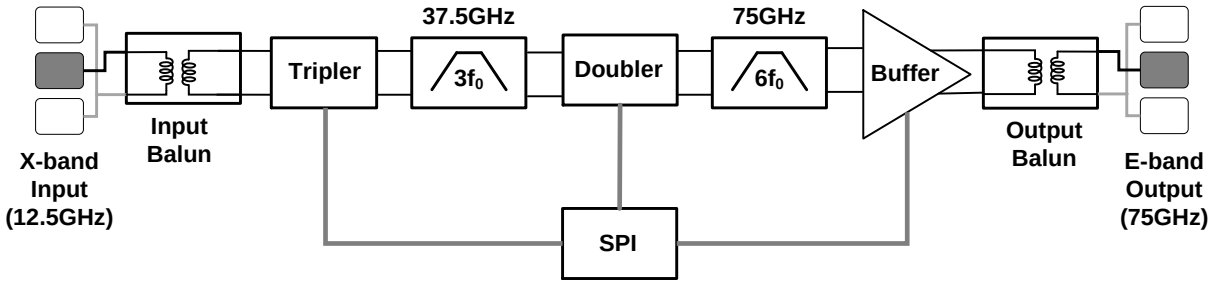

Figure 3.1. Overall arcitechture of the FMX6 chip

The input balun converts the single ended input from the X-band PLL to a differential signal which is more suitable for operation of the following blocks. Multiplication by 6 is achieved in two steps of x3 and x2 and each frequency multiplier stage is followed by a matching transformer. The buffer amplifies the E-Band doubler's output and feeds it to the output balun to have a single ended signal going outside the chip. The bias current for each bock and some other fine tunning parameters are digitally programmable through the SPI interface shown in the figure. Figure 3.2 shows a microphotograph of the chip which measures 1.71mm by 0.81mm.

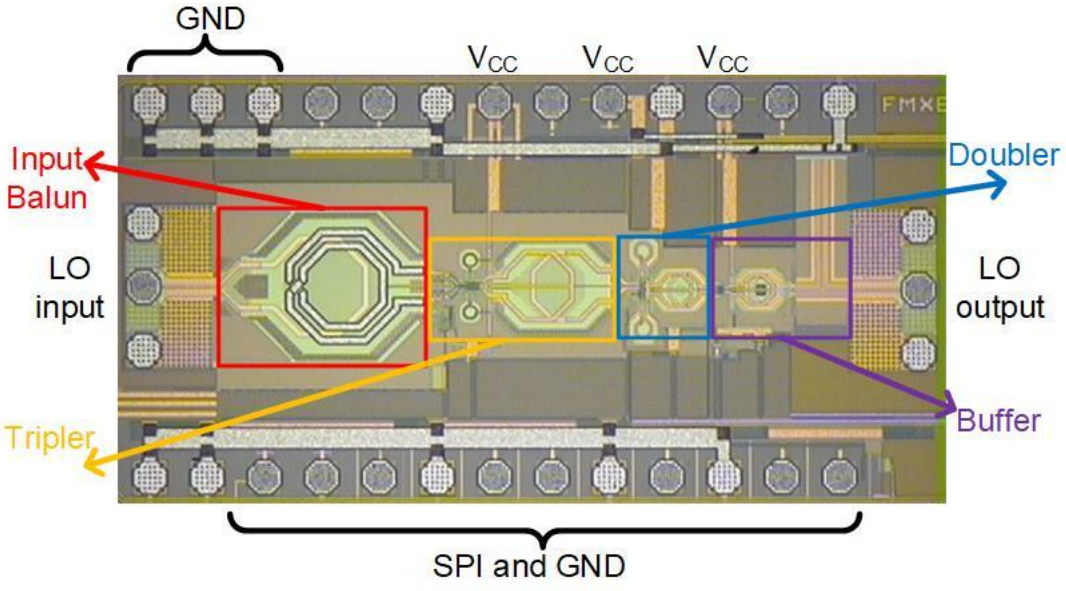

Figure 3.2. Microphotograph of the FMX6 chip

3.2 Measurement setup

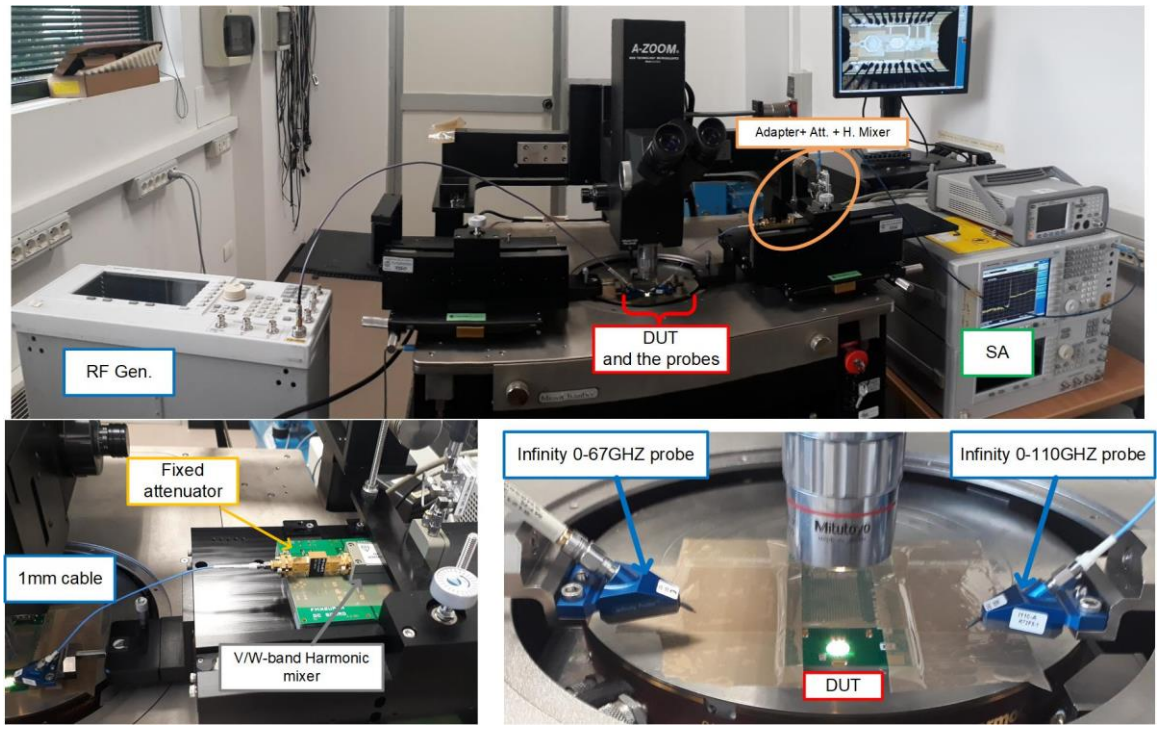

Figure 3.3. Measurement setup for the FMX6 chip

Figure 3.3 shows a few pictures of the measurement setup. An Agilent E8257D signal source was used to provide a clean signal at X-band. The sextupler's output nominally covers 70-80GHz and higher harmonics of the input signal, whose magnitude is important to measure the spectral purity of the output tone, fall at even higher frequencies. Since the Agilent N9030A spectrum analyzer can measure signal frequencies only upto 50GHz, V and W-band 11970 series harmonic mixers were used to cover the 50-75GHz and 75-110GHz bands, respectively. Moreover, since the compression point of the harmonic mixer is low (<0dBm), a 20dB fixed waveguide attenuator was placed in front of both mixers.

3.3 Measurement results

All losses of the input an output paths including the probes, cables, waveguides, adapters etc were carefully measured and de-embeded from the results. The most important characteristics of the sextupler are the output power verus frequency and input power, and also the spectral purity of the output tone. Figure 3.4 shows frequency response of the multiplier. The center frequency was slightly down shifted compared to simulations, but since the bandwidth was initially designed wider than required, it still covers the DREAM bandwidth with more than 0dBm output power with a peak of about 3.2dBm and burning about 80mW from a 1.7V supply. Moreover, all spurious tones are suppressed by more than 39dBc in the band of interest. Sensitivity of the output power to the input power variations was also investigated and the P_{out}-P_{in} curve is plotted in Figure 3.5. It can be seen that at 75GHz, P_{out} stays above 0dBm for P_{in} larger than -5dBm.

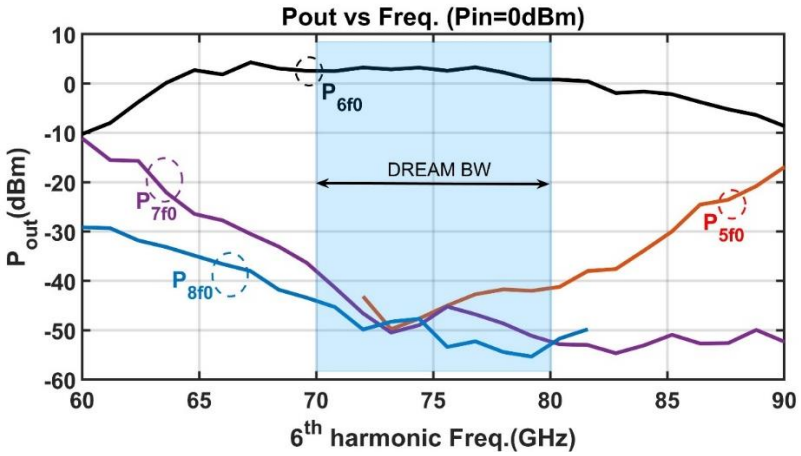

Figure 3.4. Measured output power of the 6th harmonic and the largest spurious tones versus frequency for 0dBm input signal

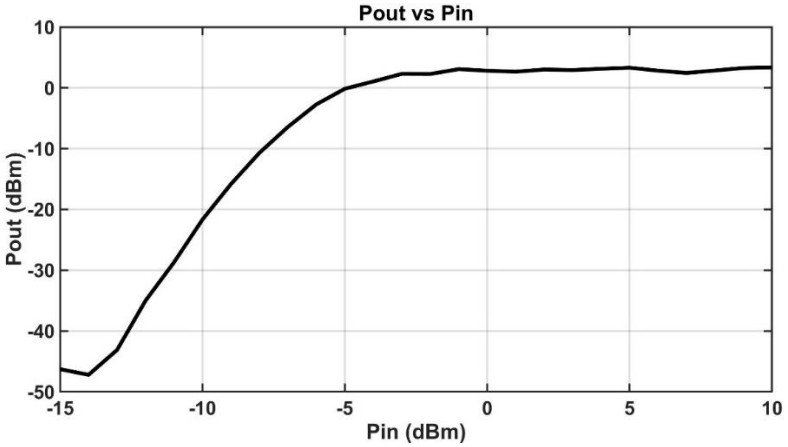

Figure 3.5. Measured output power versus input power level at center frequency

4. The D-band doubler

4.1 Chip architecture

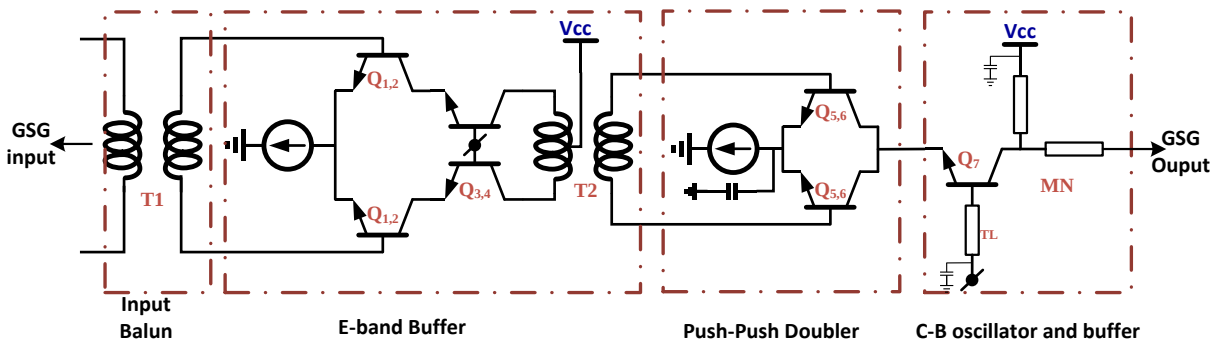

Figure 4.1. Overal architecture of the FMX2 chip

Figure 4.1 shows the overall architecture of the FMX2 chip, fully designed in STMicroelectronics BiCMOS55nm technology. The input Balun converts the single ended output of FMX6 to a differential signal which is more suitable for operation of the following blocks. The Balun is followed by an input buffer which is basically a differential amplifier working in E-band to boost the signal for the next stage, allowing operation at low input power levels. Multiplication by 2 is realised by using two parallel devices in push-push configuration. Although the push-push pair already generates the second harmonic of the input signal, it still needs amplificiation to drive the load with sufficient power. Q7, together with the transmission line at its base and its parasitic capacitances forms a common-collector Colpitts oscillator which is injection locked by the push-push pair. Hence, output of the push-push pair is buffered by the strong oscillation current of Q7. A matching network, mainly composed of transmission lines, ensures maximum power transfer to the load and also provides filtering of unwanted harmonic tones.

Not shown in this figure, the bias current of each block is digitally programmable. The programming is done by means of digital bits, provided by an integrated SPI interface. Figure 4.2 shows a microphotograph of the IP which measures 600um by 270um, including the input and outout signal pads.

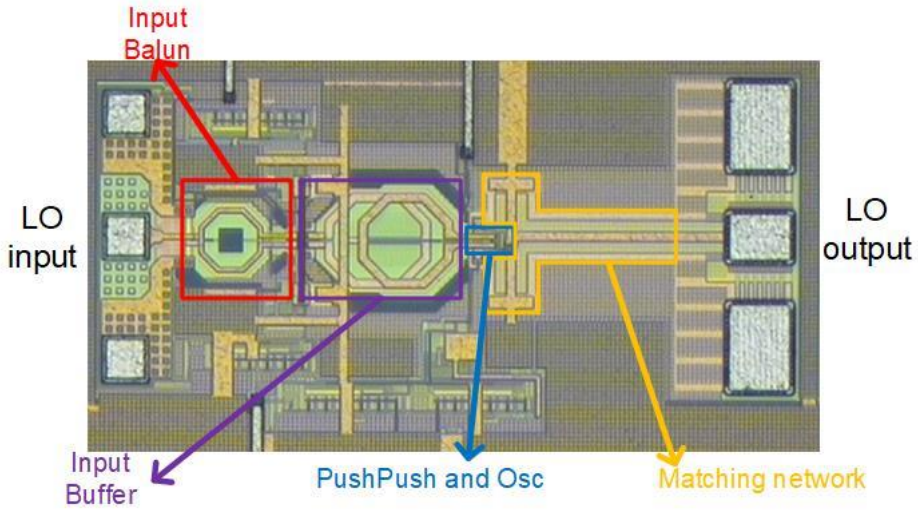

Figure 4.2. Microphotograph of the FMX2 chip

4.2 Measurement setup

A few pictures from the measurement setup are shown in Figure 4.3. Since the RF generator output is limited to 70GHz, an extension module is used. The Agilent N5260 extension module allows up-converting the input RF signal, generated by an RF generator, by a multiplication factor of 6 and covers the 67-110GHz range. By applying an LO signal and measuring the feedback signal at the reference path of the extension module at the associated IF frequency, the output power of the module can be monitored. The D-band output can be measured directly using a D-band power meter, as shown in the bottom picture in Figure 4.3 (b). However, in order to see the D-band expectrum and check the spectral content of the output signal, a VDI D-band extension module was used in receive mode. By applying an LO signal to the VDI module (through a built-in multiplication factor of 12), the input of the module is downconverted at the module's IF measure path and can be monitored on a spectrum analyzer. By sweeping the LO frequency and saving the spectrum each time, the complete D-band spectrum was reconstructed.

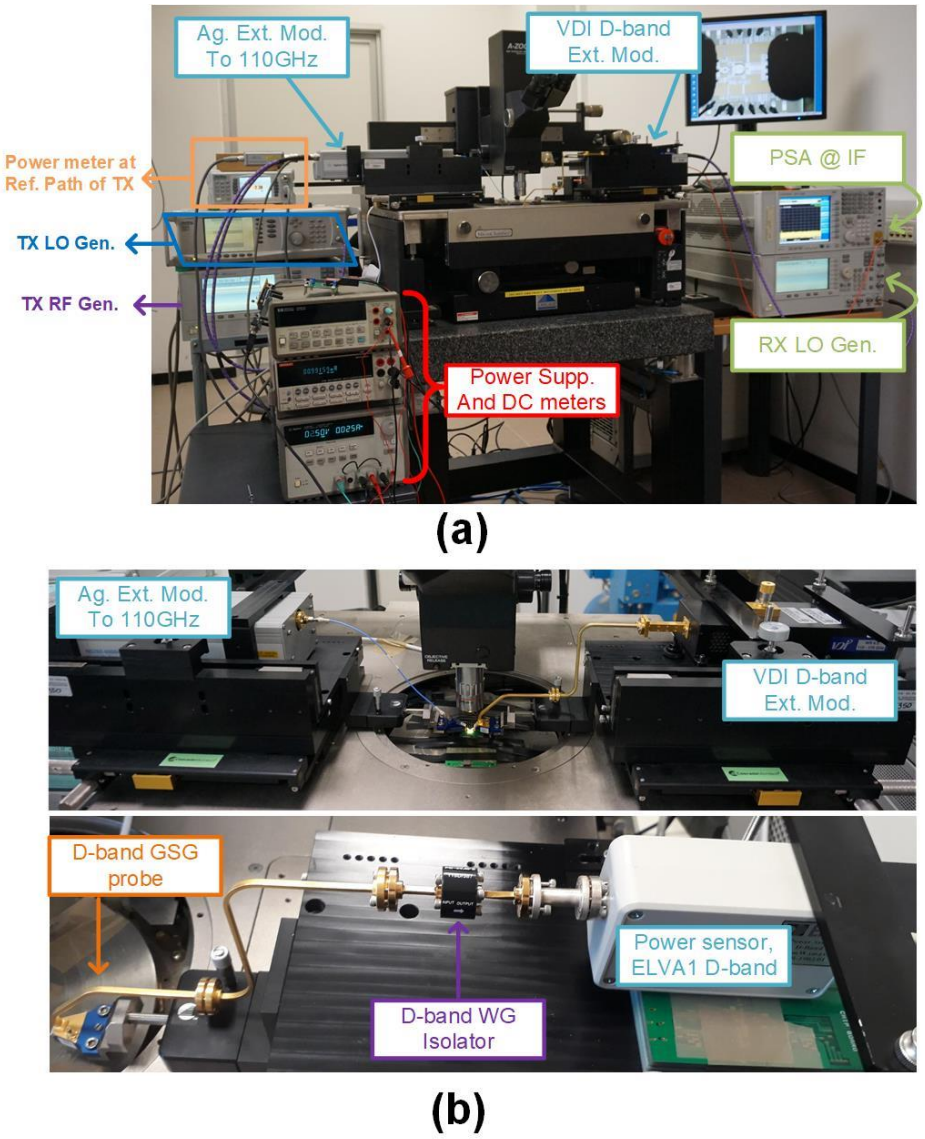

Figure 4.3. (a) Measurement top view, (b- top) Down converting the D-band output spectrum and measuring with PSA, (b-Bottom) measuring directly using power meter.

4.3 Measurement results

The doubler was designed to deliver the highest outpout power at 150GHz, the center frequency for the DREAM. However, the measurement results indicated a frequency down-shift to 130GHz. Figure 4.4 shows the measured and simulated output power versus frequency for an input power of -5dBm. Also the output reflection coefficient is depicted in Figure 4.5m where the frequency downshift is visible. The reasons for this downshift is currently under investigation, but mostly likely they arise from modelling inaccuracies of both the active and passive elements. Nevertheless, despite this frequency shift, the doubler can still be used at the initial target frequency band, 140-160GHz, as it delivers >-10dBm output power in this range which is the power level required by the following block of the transceiver chain, i.e. the LO drivers of the up/down converters. Sensitivity of the output power to the input power variations was also investigated and the P_{out}-P_{in} curve is plotted in Figure 4.6Figure 3.5. It can be ssen that at 150GHz, P_{out} is saturated with Pin less than -5dBm, whereas at 130GHz, more than 0dBm of Pout is ensured with Pin as low as -15dBm.

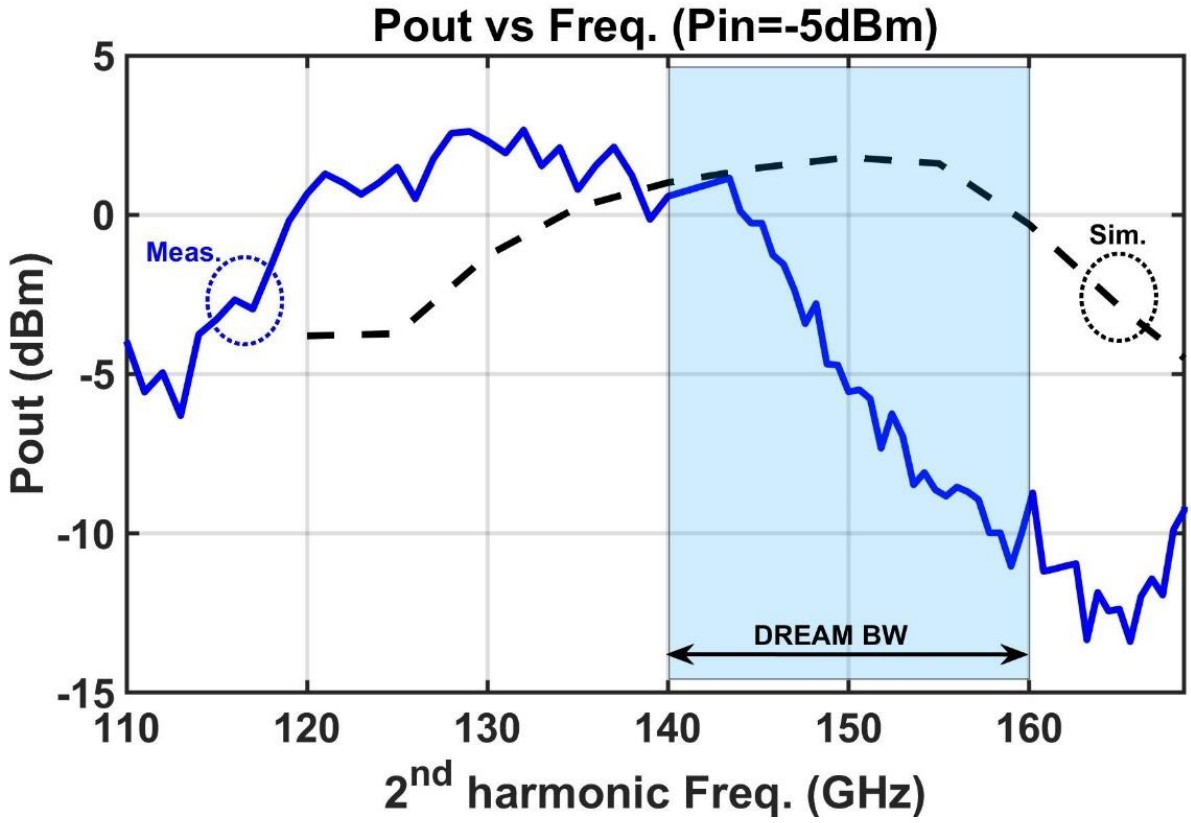

Figure 4.4. Measured and simulated output power of the D-band frequency doubler with Pin=-5dBm

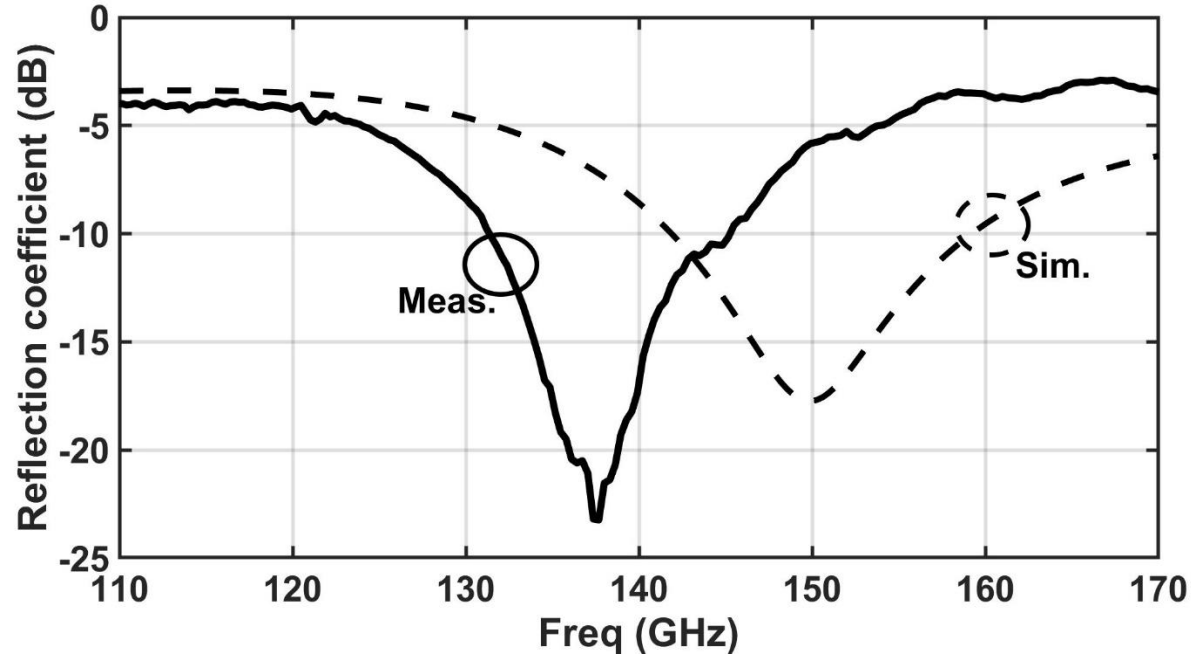

Figure 4.5. Output reflection coefficient of the FMX2

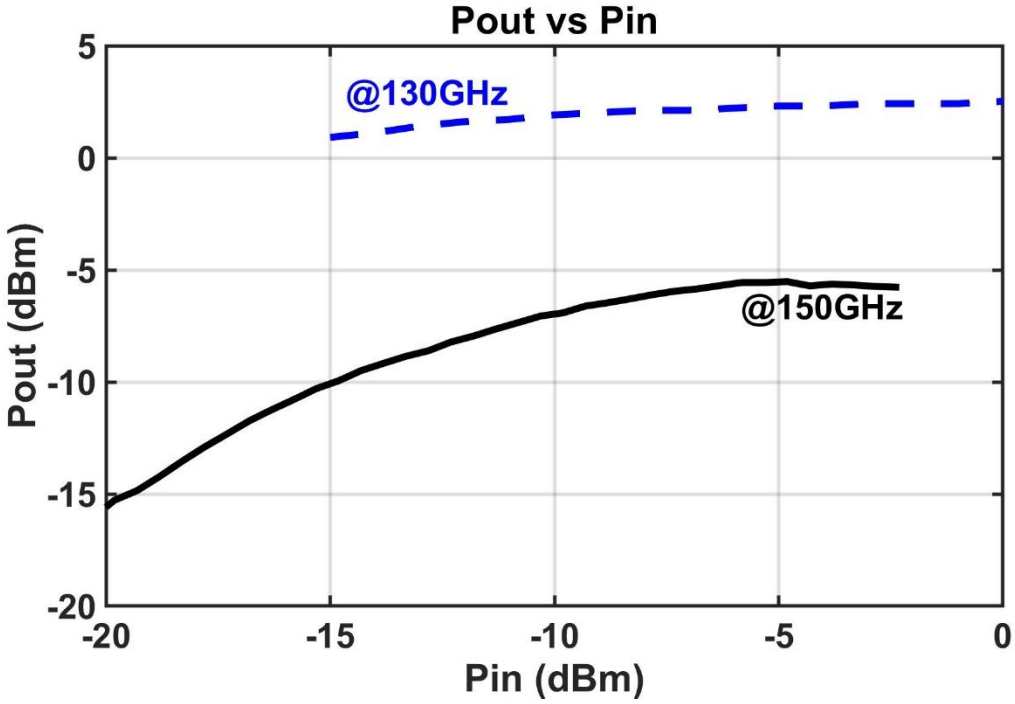

Figure 4.6. Measured output power versus input power at 130 and 150GHz.

5. Conclusions

The design specifications of the LO multiplication chips, previously reported in deliverable D.1.5 (tables 10.1 and table 5.2 for the FMX6 and FMX2 chips) are listed in Table 5.1. As shown by the numbers in the table, most of the specifications are met. The FMX6 chip, delivering output signal in E-band is very well aligned with the design target. The initial specifications are met with 3x less power consumption than planned. Measurements on the the FMX2 chip, with output in D-band, pointed out a downshift of the center frequency, from 150GHz (design target) to 130GHz (measured). The FMX2 reaches high output power and conversion gain at the measured center frequency with 4x less power consumption than initially planned. The same chip is still functional in the 140GHz-160GHz range with Pout > -6dBm (the design target) up to 150GHz. From 150GHz to 160GHz the output power gradually reduces down to -10dBm. This should not preclude testing of the demonstrator also in the upper portion of the target frequency range because, thanks to the LO buffer embedded with the I/Q converters,measurements reported in the deliverable D2.3 have shown acceptable performance also with LO power reduced to -10dBm.

Table 5.1. Comparison of expected and measured specifications of the LO chain at E and D-bands.

Parameter	Expected @ E-band	Measured @ E-band	Expected @ D-band	Measured @ D-band	Comments
Frequency range	70-80GHz	63.5 -82GHZ	140-160GHz	110-160GHz	
Power	>0dBm	3.2 – 0 dBm	>-6dBm	+2dBm to -10Bm	
Integer Spur Level	<-36dBc	<-39dBc	<-30dBc	<-30dBc	
Output reflection coefficient	NA	NA	-10dB	-23dB	Minimum, @ 137GHz
PN @ 1MHz offset	-102 dBc/Hz	NA	-96 dBc/Hz	NA	
Noise floor	-146	NA	-140	NA	
Supply Voltage	1.7	1.7	2.5	2.5	
DC current	Max. 150mA	48mA	100mA	23mA	