40GHz Frequency Tripler with High Fundamental and Harmonics Rejection in 55nm SiGe-BiCMOS

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***Abstract*— This paper presents a novel frequency tripler circuit topology which yields a remarkable improvement on the suppression of the driving signal frequency at the output, compared to conventional designs exploiting transistors in class-C. The active core of the circuit approximates the transfer characteristic of a third-order polynomial that ideally produces only a third-harmonic of the input signal. Implemented in a 55nm SiGe-BiCMOS technology and consuming 13.6mA from 1.7V, the tripler demonstrates ~40dB suppression of the input signal and its 5th harmonic over 16% factional bandwidth and robustness to power variation of the driving signal over a 15dB range.**

Keywords—mm-wave, BiCMOS, Frequency multiplier, Tripler, Harmonic rejection

I. INTRODUCTION

Communications at millimeter wave (mm-wave) have drawn a lot of attention in recent years due to the wide available bandwidth which translates directly to higher data transmission capacity [1]. Generation of the transceivers local oscillation (LO) is critical because many contrasting requirements, i.e. tuning range (TR), phase noise (PN), output power, and level of spurious tones, affect the system performance. Differently from what is commonly pursued at Radio Frequency, LO generation with a PLL embedding a VCO at the desired output frequency is not viable at mm-wave. In fact, the severe impact of device parasitics in silicon technologies, and the low quality factor of passive components (mostly variable capacitors) impair the achievable PN and TR. Moreover, traditional frequency dividers in the PLL need excessive power consumption.

A more promising approach consists of a PLL in the 10-20GHz range, where silicon VCOs feature the best figure of merit, followed by a frequency multiplier. However, the multiplier must provide good suppression of the driving signal and undesired harmonics not to impair the transceiver performance, particularly with high-order modulations [2]. In a frequency multiplication chain, the first stage must feature the highest suppression because its spurious tones are shifted close to the final LO frequency by the intermodulation of the cascaded stages. Moreover, the issue is more critical for odd-order multipliers, because even-order multipliers (e.g. frequency doublers) may exploit push-push transistors for suppression of the driving signal and its odd harmonics [3].

Odd-order multipliers, such as frequency triplers, are typically realized with a transistor with low conduction angle (class-C) that generates a harmonic rich current, and the desired tone is selected with a band-pass filter or, more efficiently, with an injection-locked oscillator. However, in both cases the total harmonic rejection ratio (HRR) is typically around 20dB [4, 5], dominated by leakage of the driving signal, with some exceptions reaching 30dB [6]. The suppression of the driving signal could be by improved by rising the filter selectivity, but at the cost of larger power consumption or bandwidth limitation.

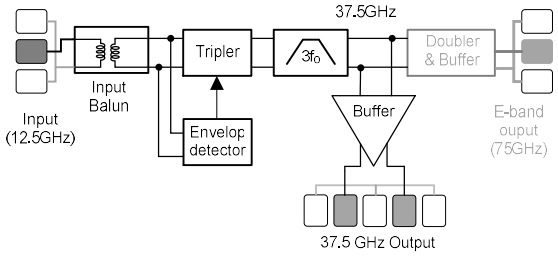

Fig. 1. Block diagram of the frequency tripler in the multiplier by 6 chain.

In this work, a novel frequency tripler circuit topology is presented which substantially improve the HRR against class-C multipliers without relying on filtering. As shown by the block diagram in Fig. 1, the tripler is followed by a doubler to form a frequency multiplier by 6 for LO generation in E-band. A very linear and broad-band buffer between the two stages allows accurate tripler characterization. Implemented in a 55nm SiGe-BiCMOS technology and consuming 13.6mA from 1.7V, the tripler demonstrates ~40dB suppression of the input signal and 5th harmonic over 16% factional bandwidth and robustness to power variation of the driving signal over a 15dB range. The paper is organized as follows: Sec-II reviews the issue of driving signal suppression in class-C triplers. The proposed solution is introduced in Sec. III while measurements are presented in Sec. IV. Sec. V summarizes the results and concludes the paper.

II. CLASS-C FREQUENCY TRIPLER

The most common method for generation of odd harmonics of a signal is by using a transistor biased in class-C, as shown in Fig. 2a. For frequency multiplication by 3, the LC load is tuned to a center frequency of $3f_0$ (being f_0 the input signal frequency). The -3dB bandwidth is inversely proportional to the filter quality factor: $BW_{-3dB}=1/Q$. The harmonic content of the transistor current, I_{out}, is set by the conduction angle, θ, determined by the bias voltage V_{bias}. To gain insight, the top plot in Fig. 2b reports the simulated fundamental (I_{f0}), 3rd harmonic (I_{3f0}) and 5th harmonic (I_{5f0}) currents, normalized to transistor area, as a function of θ. The HRR is dominated by I_{f0}, i.e. the leakage of the driving signal, which is always larger than I_{3f0}, as evident also from the bottom plot showing the ratio I_{f0}/I_{3f0}. $\theta\approx150°$ maximizes I_{3f0} and hence the tripler output

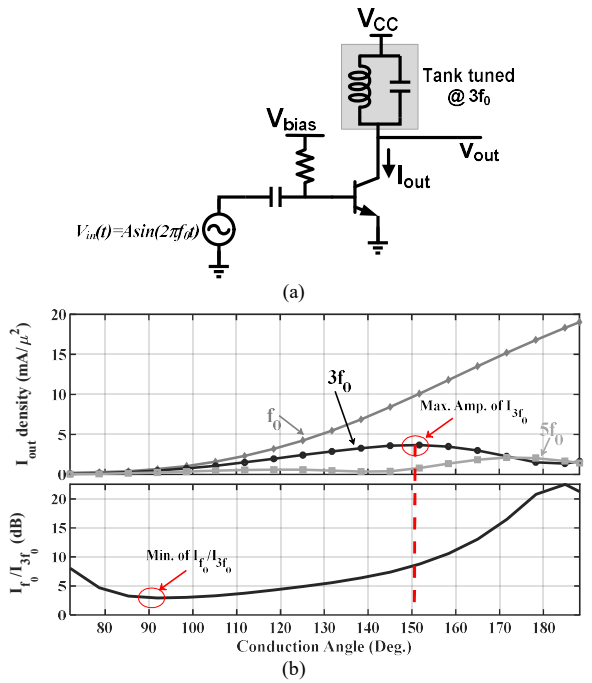

Fig. 2. (a) Single BJT biased in class-C as a harmonic generator (b) Harmonics of I_{out}.

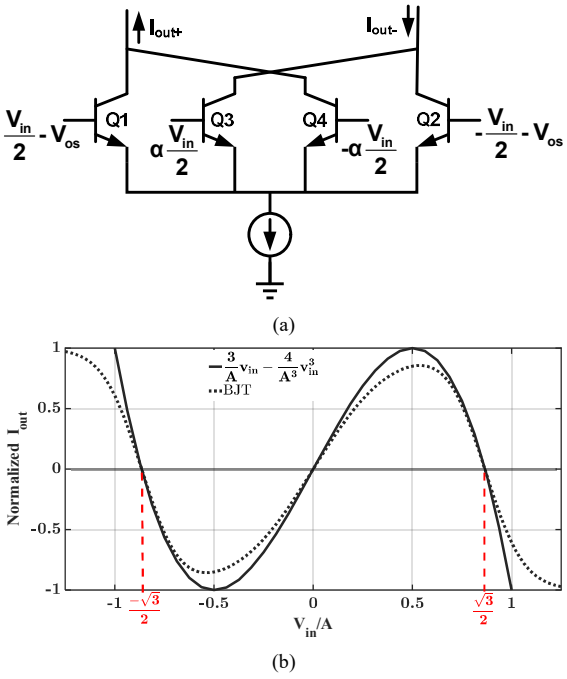

Fig. 3. (a) Simplified schematics of the proposed tripler (b) comparison of the DC transfer characteristic with Eq. (1).

amplitude but I_{f0} is 9dB larger than I_{3f0} (bottom plot). Targeting a bandwidth of 15% (Q=6.7) the rejection of I_{f0} from the LC load is 20log(3)+20log(Q)=26dB, leading to HRR=26-9=17dB only on the tripler output voltage (V_{out}). Looking again at the plots in Fig. 2b, I_{f0}/I_{3f0} is minimized (from 9dB to 3dB) at θ≈90°. This improves HRR by 6dB, from 17dB to 23dB. However, I_{3f0} at θ≈90° is roughly 5 times lower than at θ≈150°. Therefore, the mild improvement of HRR comes at the price of 14dB output amplitude reduction. In summary, despite its simplicity, the class-C tripler suffers from very poor suppression of the driving signal. The latter can be improved, in principle, by using a more complex filter topology or by cascading multiple filtering stages, but at the cost of design complexity, bandwidth limitation and power penalty.

III. Proposed Frequency Tripler

A. Principle of operation

Assuming a sinusoidal driving voltage, $V_{in}(t)=A\sin(2\pi f_0 t)$, the active core of an ideal tripler generates current only at the 3rd harmonic if the trans-characteristic follows the 3rd order polynomial:

$$I_{out} = \left(\frac{3}{A}v_{in} - \frac{4}{A^3}v_{in}^3\right) g_m \qquad (1)$$

Fig. 3a shows the proposed circuit schematic to approximate the polynomial in Eq.(1) while the ideal and approximated trans-characteristics are plotted in Fig. 3b. $Q_{3,4}$ are driven by the input signal attenuated by α. $Q_{1,2}$ are directly driven by the input signal but with a negative DC level shift ($-V_{os}$) with respect to the base of $Q_{3,4}$. The circuit operation is as follows: at small V_{in}, the lower bias voltage keeps $Q_{1,2}$ off and the circuit approximates eq.(1) near the origin with a simple differential pair formed by $Q_{3,4}$. But when V_{in} rises, $Q_{1,2}$ turn on, subtract current from the outputs and reverse the slope of the trans-characteristic. The zero crossings of the current offsetted from the origin (in Fig. 3b), occur when the voltage at the base of $Q_{3,4}$ equals the voltage at the base of $Q_{1,2}$ i.e. $\frac{1}{2}\alpha V_{in}=\frac{1}{2}V_{in}-V_{os}$. This condition is satisfied for $v_{in} = \pm 2V_{os}/(1-\alpha)$. The zero crossings of eq.(1) are at $v_{in} = \pm\sqrt{3}A/2$. Therefore V_{os},α must be selected to satisfy:

$$\frac{2V_{os}}{(1-\alpha)} = \frac{\sqrt{3}}{2}A \qquad (2)$$

Further circuit analysis proves that setting α=0.2 allows to fit the slope of eq.(1) near the three zero crossings. With α fixed, eq.(2) shows that to maintain the correct zero crossings at different input power V_{os} must be varied linearly with the input signal amplitude (A). Therefore, V_{os} is generated by an envelope detector, shown in the block diagram of Fig. 1.

Looking at the plot in Fig. 3b, the transistor implementation approximates very well eq.(1). Simulations at low frequency confirm that the circuit suppresses almost completely the component at f_0 in the output current. With a driving signal in Ku-band, device parasitic capacitors distort the dynamic shape of the trans-characteristic and reduce the f_0 suppression, but the issue can be solved by resonating out the equivalent shunt capacitance at the common-emitter node at frequency $2f_0$. The achievable f0 rejection is ultimately limited by the accuracy to which V_{os} is set.

B. Circuits Design

The complete tripler circuit is shows in Fig. 4. The differential signal provided by the transformer balun (T_1) drives directly the base of $Q_{1,2}$ while it is attenuated by α through a capacitive voltage divider (C_1, C_2) to feed the base of $Q_{3,4}$. The four transistors have the same emitter area

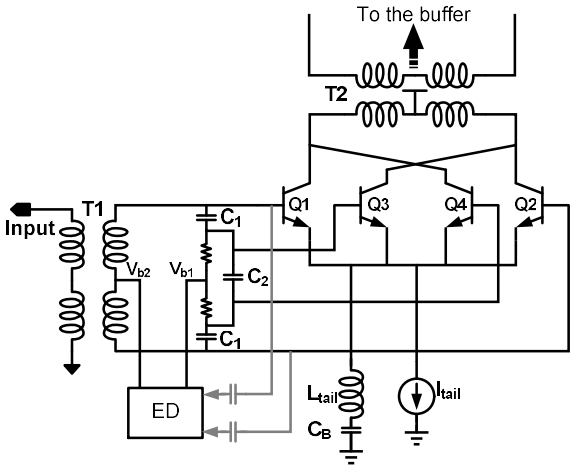

Fig. 4. Detailed schematics of the proposed Tripler.

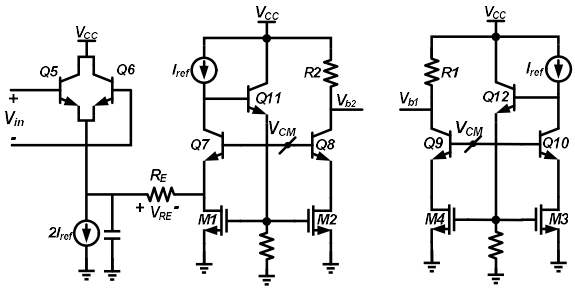

Fig. 5. The Envelope detector Circuit.

(A_e=17.5x0.2 um^2) and biased by I_{tail}=12.8mA. The inductor L_{tail} resonates with the equivalent shunt capacitance at the common-emitter node and C_B is sized sufficiently large to act as an AC short. The quality factor of L_{tail} is not critical, because the impedance at resonance is limited by the low equivalent resistance at emitters of $Q_{1\text{-}4}$. The transformer T_2 provides the supply voltage (V_{cc}=1.7V) and couples the tripler to the cascaded circuits (test buffer and doubler, shown in Fig. 1). The transformer is designed to achieve a fractional bandwidth of 16%, centered at 37.5GHz.

V_{b2} and V_{b1} are the bias voltages for $Q_{1,2}$ and $Q_{3,4}$ respectively. They are generated by the envelope detector (ED) block such that V_{b1}-V_{b2} (corresponding to V_{os} in Fig. 3) tracks the amplitude of the driving signal. The ED circuit schematic is shown in Fig. 5. $Q_{5\text{-}10}$ share the same bias voltage, V_{CM}. In this way, $Q_{5,6}$ (driven by $V_{in}(t)$) and Q_7, set V_{RE} equal to the average value of $|V_{in}(t)|$. If $V_{in}(t)=A\sin(2\pi f_0 t)$, $V_{RE}=(4/\pi)A$ and $I_E=(4/\pi)A/R_E$. $M_{1,2}$ mirror $I_{ref}+I_{RE}$ into R_2 while $M_{3,4}$ mirror I_{ref} into R_1 leading to $V_{b2}=V_{cc}-(I_{ref}+I_{RE})R_2$, $V_{b1}=V_{cc}-I_{ref}R_1$. Assuming $R_1=R_2$ results in $V_{os}=V_{b2}-V_{b1}=R_2\ I_{RE}=(4/\pi)(R_2/R_E)A$. The ratio R_2/R_E is designed such that V_{os} satisfies eq.(2), thus allowing to maintain good suppression of the fundamental frequency component independently from the amplitude of the input signal.

The buffer in the block diagram of Fig. 1 is designed with the purpose of performing accurate experimental characterization of the tripler circuit. It is realized with a resistively degenerated cascode differential pair with resistive load and peaking inductors. From simulations, the buffer attenuates by 9.6dB with 70GHz bandwidth, allowing

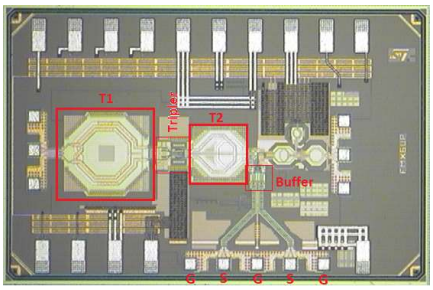

Fig. 6. Chip photograph

measurements up to the 5th harmonic of the input. The output power at 1dB gain compression point is 1dBm.

IV. Measurement Results

The frequency tripler is designed and fabricated in ST Microelectronics 55nm SiGe-BiCMOS technology. The chip photograph is shown in Fig. 6. The input signal is provided by a CW source and the output is measured using a spectrum analyzer. The on-chip buffer provides a differential output (GSGSG pad in Fig. 6) but measurements are performed single-ended by probing each of the two outputs separately. Fig. 7 compares the measured and simulated power delivered to a 50Ω load at $3f_0$ and leakage of f_0 and $5f_0$ versus frequency when the tripler is driven by a 0dBm input signal. The single-ended peak output power is 0dBm at 37.8GHz and remains within 3dB variation from 35 to 41GHz, corresponding to 15.8% fractional bandwidth. Maximum and minimum rejection of f_0, $5f_0$ in this frequency range are 43.8dB and 37.5dB respectively. The second harmonic ($2f_0$) present in single-ended measurements remains 45dB below the desired signal. The tripler and ED draw 13.6mA from a 1.7V supply while the output buffer, not optimized for power efficiency but for wide bandwidth and high linearity, draws 32mA from a 3V supply. From simulations, the differential voltage swing at the buffer's input is around 930mV zero-peak.

Fig. 8 shows the measured output power at $3f_0$ when the input power is swept at 12.5GHz. The same plot reports the HRR considering signal leakage at f_0 and $5f_0$. In the range –5 to 10dBm the single-ended output power at 3_{f0} rises from -8 to +4dBm. The HRR is better than 40dB until 4dBm input power and reaches 36.6dB for 10dBm input.

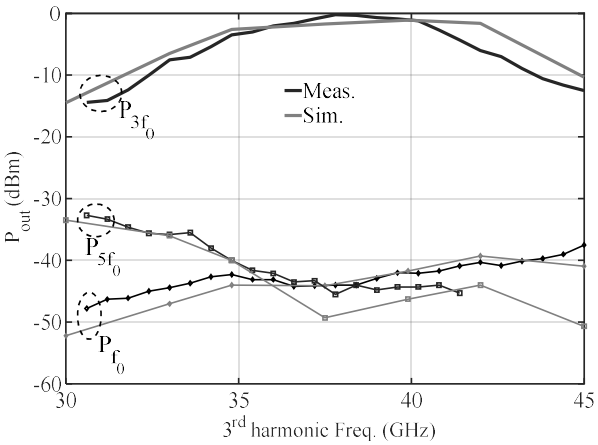

Fig. 7. Measured output power of the 3rd harmonic, f_0, and f_5 leakage versus frequency for 0dBm input signal.

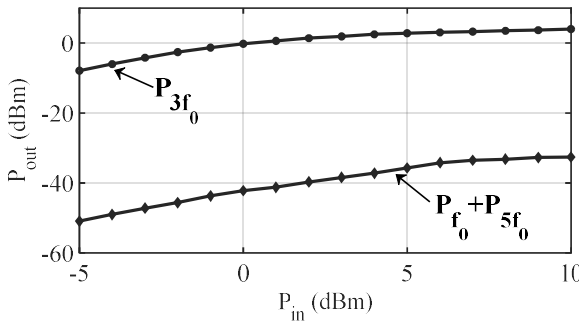

Fig. 8. Measured output power of the 3rd harmonic and HRR versus input power at f_0=12.5GHz

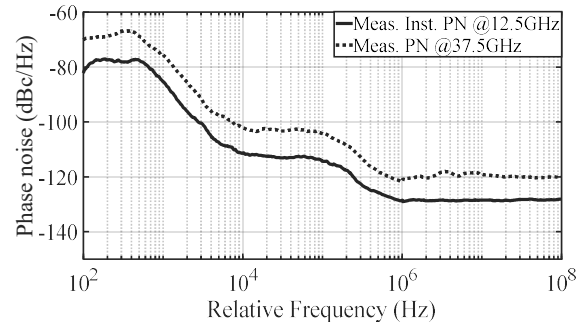

Fig. 9. Phase noise performance

Fig. 9 shows input and output PN at 12.5GHz and 37.5GHz, respectively. The difference between the two plots is 9.5dB, as expected by the frequency multiplication by 3, thus proving negligible phase noise deterioration from the tripler.

Finally, measurement results are summarized in Table I and compared against previously reported frequency triplers. All the designs are based on transistors in class-C for harmonic generation. On average, the rejection of unwanted tones is near 20dB. [6] reaches 33dB by leveraging injection locking filtering, but at the cost of narrow bandwidth, limited by the locking range. The tripler in [5] reaches 28dB rejection and maintains wide bandwidth by inserting a notch filter tuned to f_0, but the core power dissipation is nearly 3 times larger than in this work. The proposed solution demonstrates > 10dB improvement of undesired harmonic tones rejection with operation bandwidth and core power dissipation aligned with state of the art.

V. Conclusion

A novel frequency tripler for mm-wave LO generation has been presented. The active core is devised to reproduce the trans-characteristic of a 3rd order polynomial that ideally generates only the 3rd harmonic of a sinusoidal input signal. By leveraging an envelope detector to set the correct bias voltage, the circuit maintains high suppression of the driving signal and 5th harmonic over wide variation of the input amplitude. Implemented in a 55nm SiGe-BiCMOS technology with 23mW core power dissipation, the circuit demonstrated the highest reported suppression of the input signal and 5th harmonic over 16% factional bandwidth and robustness to input power variation over a 15dB range.

TABLE I. Measurement summary and comparison

Ref	*Tech*	*f_{out} (GHz)*	*Supp. of Largest tone (dBc)*	*P_{in}/P_{out} (dBm)*	*P_{DC} (mW) Core + Buffer*
[7]	0.18um SiGe BiCMOS	80-100 (20%)	20	0/-10.5	5+70
[6]	65nm CMOS	85-95.2 (3.5%)[a]	32.9	4/-3.8[b]	5.2+ 14.6
[8]	0.13um CMOS	57-61 (6.6%)	22-31.3	0.5/-9.5	9.96+16.1
[9]	0.15um PHEMT	58.5-65 (10.5%)	19-21	-1/-2.6	56
[5]	0.13um SiGe	48-58 (19%)	28-38	-2.5/9.5	62+158
[10]	0.13um CMOS	36-48 (28%)	10-40	0/-11.4	12.6+11.9
[11]	0.15um PHEMT	35-38.5 (9.5%)	10-22	9/-0.4	18.9
This work	0.18um SiGe BiCMOS	35-41 (15.8%)	37.5-43	0/0 (Single ended)	23+96

[a] Widest locking range reported

[b] Differential output

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