Design of Integrated Control Circuits for mm-Wave Phased Arrays in 55-nm BiCMOS

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***Abstract*—This paper presents the design of different control circuits for integrated D-band phased-array transceivers, implemented using a 55-nm BiCMOS process. An SPI slave controller is first presented, which is able to control a bank of sixteen 8-bit registers. The design of an integrated ring-oscillator based clock generator is then described, which oscillates at 44 MHz. Finally, a current-steering 8-bit DAC is presented, which provides a current of 0-1.8 mA with a DNL lower than 0.9 LSB. The DAC can be used to generate bias currents for mm-wave phase shifters and amplifiers, as well as to generate self-test signals at a sampling frequency of up to 100 MSPS. The clock and DAC have been implemented on a test chip that occupies 0.5 mm x 0.4 mm.**

I. Introduction

The data rate demanded by the users in mobile communications has increased exponentially in the last decades. This trend is expected to follow for 5G and beyond, where Gbit/s data rates are envisioned for single users. Providing such data rates poses new challenges to the network infrastructure, especially when a radio solution is used within this network infrastructure [1]. A radio backhaul transport network working close to the access part is expected to satisfy [2], [3], [4]:

- Capacity up to 100 Gbit/s (50 Gbit/s uplink plus 50 Gbit/s downlink)
- Availability better than 99.9 %
- Latency below 0.1 ms

In order to meet the high capacity requirement, a combination of high-order quadrature amplitude modulation (QAM) with spatial diversity technology (LoS-MIMO) and, above all, very large bandwidth is needed. The required extra-wide bandwidth is only available in the high millimeter-wave region [4], [5]. The D-Band, which offers a vast bandwidth available in the range 130 to 170 GHz, is being considered as a potential candidate for the above high capacity backhaul links. An advantage of working in the high millimeter-wave region such as D-Band is that phased-arrays with a compact size and form factor can be designed. Thus, the transceiver can include a beam-steering functionality. This beam-steering feature can be used to relax the capacity/availability requirements of each single radio connection, as a configurable meshed network can be implemented to re-arrange and backup the links when necessary.

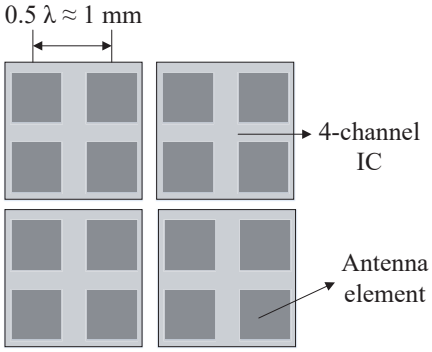

Fig. 1: 4-channel IC feeding an antenna sub-array.

The design of circuits for the high millimeter-wave region has been traditionally faced using GaAs technology, but this technology is not as well suited for the integration of complex functions and digital interfaces in the same chip as CMOS based technologies. On the other hand, the progress in CMOS technologies, and specially in BiCMOS, is pushing the limits of these technologies to ranges able to cope with the high millimeter-wave wireless communications requirements [6], [7]. Using these advanced CMOS/BiCMOS technologies, designers can embed together with high millimeter-wave analog circuits complex functionalities for control and monitoring in the same chip.

This paper presents the design of control circuits for the ICs of a phased-array operating in D-Band, implemented using a 55-nm BiCMOS technology. The paper is organized as follows. Section II describes the proposed architecture for a phased-array transceiver, section III presents the design of an SPI slave controller for the interface of the ICs, section IV deals with a clock generator for the SPI controller and section V describes a DAC that can be used to control the phase shifters and other circuits of such a phased-array transceiver. Finally, section VI concludes the article.

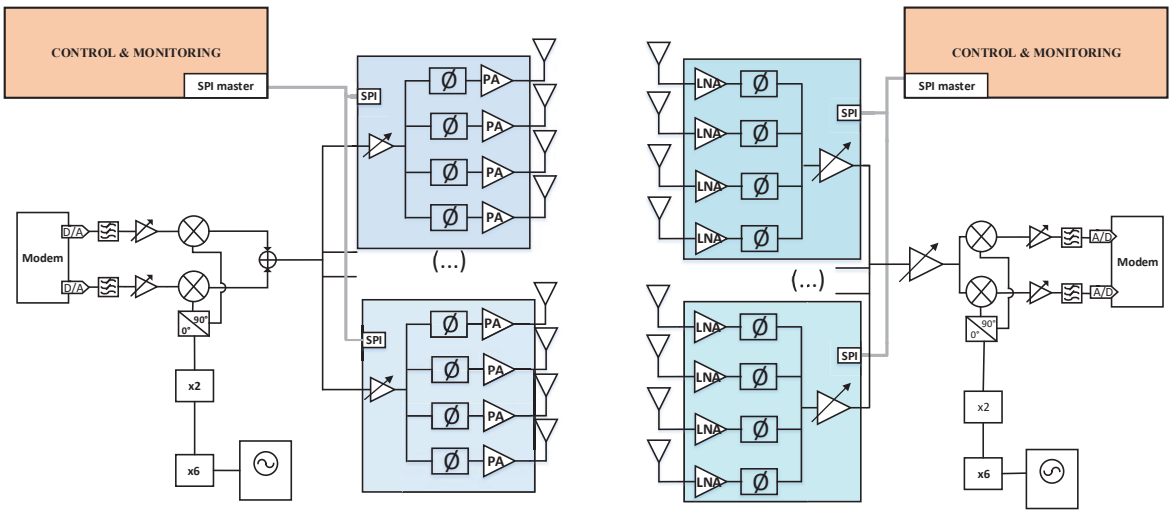

Fig. 2: Block diagram of the considered mmW phased-array transceiver.

II. System Architecture

A D-band phased-array transceiver with the architecture shown in Fig. 2 is proposed in this work. It consists of a direct-conversion transceiver, where the phase shifting is performed directly at RF. This architecture is preferred over phase shifting at baseband or at the LO chain because it makes a more efficient use of the RF front-end, simplifies the beam steering algorithm and facilitates the routing of the baseband and LO signals [8], at the cost of making the design of the phase shifters more challenging. In order to minimize the effect of the phase shifter loss on the system output power and noise figure, the phase shifters in the transmitter and receiver chains are placed before the PA and after the LNA, respectively.

The transceiver is aimed at feeding a matrix of NxN antenna elements, each connected to one PA/LNA. The followed approach is to integrate a sub-array of 4 channels in each chip, which balances the chip-level power requirements and allows compensating the loss of 4-way splitters/combiners with moderate-gain amplifiers. In addition, this arrangement allows scaling the system to address bigger arrays with 16, 64 or more antenna elements by employing more samples of the same chip.

The chip-antenna interface in a phased-array system is challenging at mm-wave frequencies, as it is important to minimize its loss and make the lengths of all the connections equal. For this purpose, the beamforming chips should be placed at the back side of the low-loss substrate containing the antenna array, connected using advanced flip-chip assemblies and low-loss vias. This means that the chips should fit into the antenna array spacing, as shown in Fig. 1. The optimum antenna spacing to avoid grating lobes is half a wavelength [9], which is 1 mm at 150 GHz. This limits the chip size and the maximum pad number, preventing the use of separate pads to access all the tuning knobs required to independently control all the amplifiers and phase shifters. Hence, integrated control circuits that provide the required flexibility and accuracy, but at the same time reduce the number of required pads, are highly desired. An SPI interface has been selected to address this, as it allows controlling a big number of registers at a high speed by using only 4 wires. By integrating an SPI slave controller and high-accuracy DACs on the chip, the desired requirements are met.

A 55-nm BiCMOS process from STMicroelectronics has been selected for this work [10]. Not only does this process provide high-performance bipolar transistors with transition frequencies above 300 GHz, but it provides the high-performance integration capabilities of a 55-nm CMOS technology as well. Therefore, it allows integrating the control circuits presented in this paper together with the mm-wave blocks of the envisaged phased-array transceiver.

III. SPI slave controller

As it has been said, an SPI interface has been selected to control and monitor the different chips and blocks in the envisaged phased-array system. The proposed approach is to include SPI slave controllers in the different chips and control them from an SPI master implemented on a microcontroller, as shown in Fig. 2. This configuration allows sharing the same SPI bus among the different chips, except for the chip select line, which needs to be different for each chip. This way, it is possible to include identical SPI slaves in all the chips to be controlled, as opposed to other interfaces as I^2C which would require setting unique addresses for each of them –usually done using integrated memories or specific hardware connections.

Fig. 3 shows a block diagram of the SPI slave controller designed in this work. It includes the standard signal pins

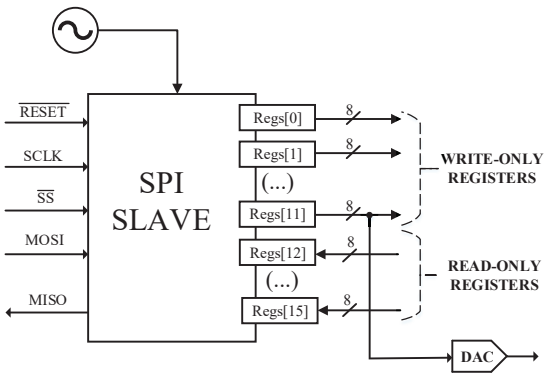

Fig. 3: Block diagram of the SPI slave.

for the SPI communication (MOSI, MISO, SCLK and SS) and it is connected to a bank of sixteen 8-bit registers. The first 12 registers are set as WRITE-ONLY registers, while the last 4 are set as READ-ONLY registers. The WRITE-ONLY registers are those to be used to control different parameters of the phased-array circuits such as the bias currents, gain of amplifiers or the phase shift, among others. They can be used directly connected to control switches or to set analog currents/voltages if connected to an integrated DAC like the one described in section V below. As for the READ-ONLY registers, they can be used to monitor different parameters of the integrated circuits such as current values, temperature or response to self-test signals.

The SPI slave controller has been designed as a synchronous block, and therefore it requires a clock signal working at higher frequency than the SPI communication speed. The design has been first described in VHDL and validated in an FPGA, by sending from an SPI master commands to write all the 0-255 words in all the registers and checking that the results were as expected. An ASIC implementation in the employed 55-nm BiCMOS process has been synthesized afterwards. The layout of the circuit occupies 85 μm x 85 μm and it works from a 1.0-V supply. The circuit has been simulated at transistor level after extracting all the parasitics from the synthesized layout. For the test, SPI control signals to write several words in the different registers were introduced in the time domain simulation, verifying that the results were correct. In the following sections the integrated clock generator and a DAC to be connected to this SPI will be presented.

IV. Clock Generator

A ring-oscillator based clock generator has been selected for this work, due to its low power consumption and compact layout. Ring oscillators are also known to have strong sensitivity to PVT variations and considerable phase noise [11], but this is not a problem in the considered application as long as the oscillation frequency is maintained below the maximum operation frequency of the implemented SPI slave (120 MHz) and well above the communication

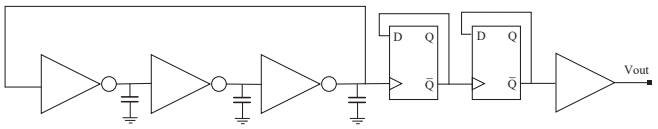

Fig. 4: Block diagram of the implemented clock generator.

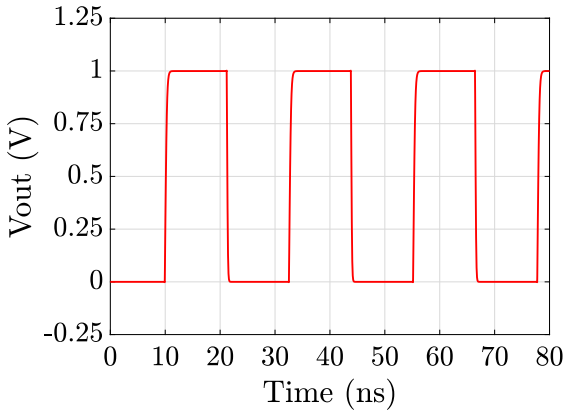

Fig. 5: Output waveform of the clock generator.

rate of the SPI interface (typically below a few MHz). A diagram of the designed clock generator is depicted in Fig. 4. It is based on a three-stage inverter ring oscillator, loaded with 150-fF MOM capacitors and followed by a divide-by-4 circuit in order to operate in the frequency range allowed by the SPI slave.

Fig. 5 shows the post-layout simulated output voltage of the clock generator, which oscillates at a frequency of 44 MHz. When simulated at PVT corners, the oscillation frequency is between 29 and 86 MHz, which falls into the range allowed by the implemented SPI slave. The layout of the circuit occupies 25.4 μm x 14 μm and draws a typical RMS current of 105 μA from a 1.0-V supply.

V. DAC Circuit

A phase shifter is an essential building block of an integrated phased-array system, as it is used to control the

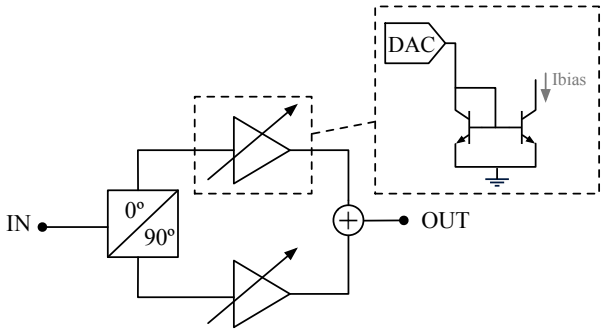

Fig. 6: Bias control circuit of a mm-wave phase shifter.

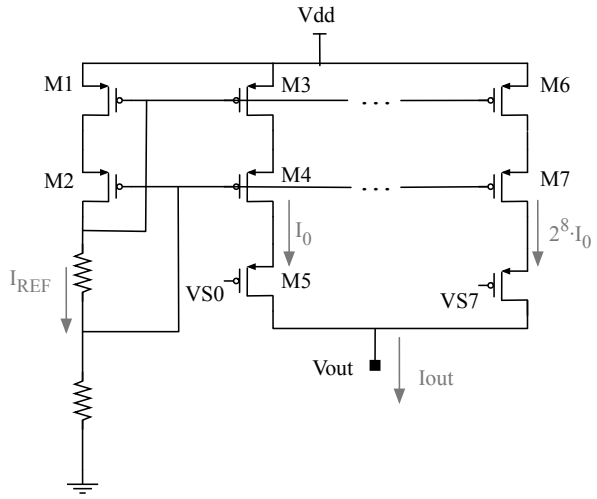

Fig. 7: Schematic of the designed DAC.

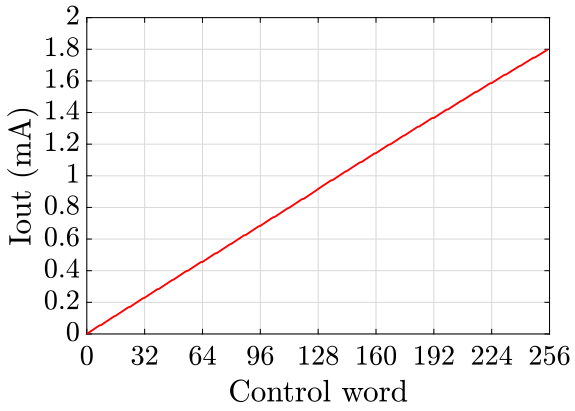

Fig. 8: Output current of the DAC.

gain and phase of the signal feeding the different antenna elements and thus, the radiation beam of the antenna array. Fig. 6 shows the block diagram of an active mm-wave phase shifter, typically based on a vector modulator [12]. By controlling the gain of two VGAs fed by a quadrature signal and adding/substracting their outputs, it is theoretically possible to implement any phase shift. A DAC can be used to control the bias current of each VGA, and consequently change their gain. With a resolution of N bits in each DAC and 2 extra bits to select the quadrant, it is possible to set $4 \cdot N^2$ different phase/gain states. For this work, it has been decided to implement an 8-bit DAC, which matches the register size of the SPI described in section III. With a pair of 8-bit DACs, each connected to one of the quadrature VGAs, it is possible to achieve 262,144 different configurations for the phase shifter, which is enough even for the most demanding applications.

The schematic of the designed DAC is depicted in Fig.7. It is based on a binary-weighted, 8-bit current-steering architecture, which is well-known to balance speed, power consumption, area and accuracy [13]. In addition, this DAC type inherently operates in current mode and therefore it can be directly used to adjust the bias current of amplifiers using simple current mirrors. In order to provide low sensitivity to the supply voltage, cascode-type PMOS current mirrors are used in the design, at the expense of a reduced voltage swing. PMOS switches are placed to select the different binary-weighted current contributions, up-sized towards the MSB to reduce voltage overhead and improve the linearity.

The post-layout simulated output current of the DAC with an 800-Ω load is shown in Fig. 8, ranging from 0 to 1.8 mA with good linearity. The calculated differential non-linearity (DNL) is shown in Fig. 9, which exhibits values lower than 0.9 LSB. This DAC is used to control the bias current of the quadrature branches in a 150-GHz phase shifter, obtaining for each branch a gain variation of -39 to -4.4 dB in 256 steps as shown in Fig. 10 (at room temperature of 25°C). When the temperature is varied between -40°C and 85°C, the maximum achievable gain varies between -2.3 and -5.6 dB, as shown in Fig. 10. This variation is mainly caused by changes in the performance of the HBT transistors building up the amplifiers, but the DAC is still capable of controlling its gain in the entire range. Therefore, it can be concluded that the presented DAC is suitable to control a phase shifter based on a vector modulator.

In addition, the performance of the DAC when generating a sinewave has also been assessed. Fig. 11 shows the post-layout simulated spectrum of the DAC output (with an 800-Ω load) when synthesizing a 1.56-MHz tone sampled at 100 MSPS, exhibiting a SFDR of 32 dB. This validates the use of the presented DAC for generating high-speed signals as well, useful for eventual fully-integrated self-test systems.

The presented DAC has been implemented in the chip shown in Fig. 12, which also includes the previously described clock generator. The manufactured circuits will be tested prior to their integration with the rest of the blocks in a fully-integrated phased array chip.

VI. Conclusion

The designs of different control circuits for an integrated D-band phased array transceiver have been presented in this paper. In particular, an SPI slave controller, a 44-MHz clock generator and an 8-bit current-steering DAC have been presented, implemented using a 55-nm BiCMOS process. The designs fulfill the requirements for highly-integrated mm-wave phased array systems and they will be integrated together with the mm-wave phase shifters and amplifiers at a later stage.

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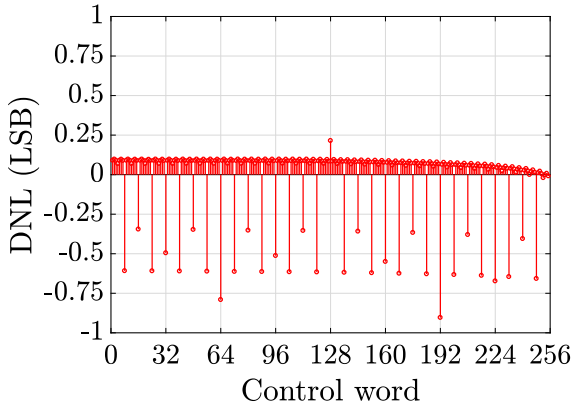

Fig. 9: DNL of the DAC.

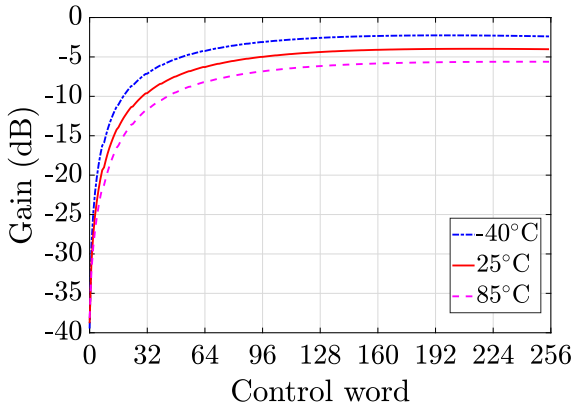

Fig. 10: Gain in a branch of a 150-GHz phase shifter as a function of the DAC control word.

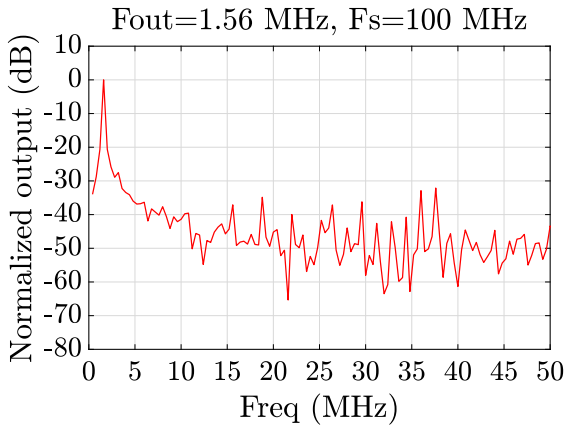

Fig. 11: Output spectrum of the DAC when generating a 1.56-MHz sinewave.

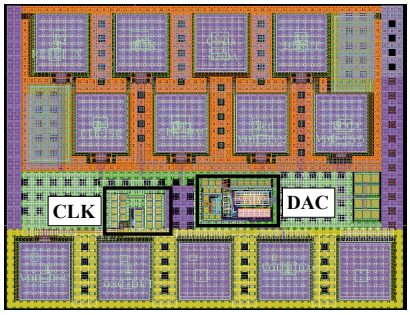

Fig. 12: layout of the test chip. Size: 0.5 mm x 0.4 mm

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