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Patch Antenna and Antenna Array on Multilayer High-Frequency PCB for D-band

Antti Lamminen, Jussi Säily, Juha Ala-Laurinaho, Jesus de Cos, Vladimir Ermolov

Abstract— **This paper presents the design, manufacturing, and characterization of a wide-band cavity-backed aperture-coupled patch antenna and a 16-element antenna array on multilayer printed circuit board (PCB) targeted for D-band applications. Microstrip line and grounded coplanar waveguide (GCPW) transmission lines are also designed and tested to investigate line losses at D-band. The test structures are manufactured using printed circuit board technology with semi-additive processing (mSAP) of conductors on a multilayered substrate. The measurement results indicate an insertion loss of 1.9 dB/cm for the microstrip line and 1.8 dB/cm for the coplanar waveguide at 150 GHz. The measured maximum gains for single antenna and 16-element array are respectively 7 dBi and 14 dBi at 143 GHz. The measured antenna input matching bandwidth is 20 GHz. The results show the viability of advanced printed circuit technology for D-band transmission lines, antennas, and antenna arrays.**

Index Terms—**D-band, antennas, antenna arrays, mSAP**

I. Introduction

SUITABLE antenna-in-package technologies for D-band applications are, for example, low temperature co-fired ceramics (LTCC) [1], integrated passive devices (IPD) [2], and thin-film processing on alumina substrate [3]. LTCC provides multilayer metal structure but is not a cost-effective solution in large scales. IPD technology enables one or more conductive layers inside polymer films on top of a carrier substrate but the layer thickness and the number of layers is usually limited [2], [4]. Thin-film processes usually only have a single patterned layer over a ground plane layer, i.e., the passive structure such as an antenna is on top of a silicon, alumina or quartz substrate. Such processes are not feasible for complex integrated systems like phased antenna arrays. An on-chip end-fire antenna in D-band has been manufactured on SiGe BiCMOS process in [5] by exploiting a localized back-side etching (LBE) feature to improve the antenna efficiency. On-chip antennas are of interest because the antenna can be integrated with the active circuitry without having lossy interconnections. However, the needed LBE makes the manufacturing complex.

Polytetrafluoroethylene (PTFE)-based substrates have been used in printed circuit board (PCB) to satisfy interconnect and antenna functions, for example, in the 77-GHz radar front-end sensors [6]. PTFE is a good candidate for millimeter-wave applications given its dielectric-constant stability and dielectric-loss properties. However, a disadvantage of PTFE is its low mechanical strength. When multiple layers of low-loss substrate are required, PTFE's low surface-energy along with its chemical resistance makes the fabrication of PTFE multilayer PCBs a difficult and expensive proposition.

In recent years, low-loss multilayer solutions have become available [7]. An example is the use of LCP (Liquid Crystal Polymer) which is a thermoplastic as PTFE. However, LCP suffers from inconsistent material movement that complicates the PCB fabrication process, particularly where feature-to-feature accuracy is of a prime consideration. As an example, a D-band grid antenna on LCP was demonstrated in [8]. A 0.5-mm thick copper sheet was needed as a core to ensure the rigidity of the two-layer LCP, which increases the manufacturing cost.

A cavity-backed patch antenna design is chosen as an antenna topology in this work. The main advantage of the cavity-backed design is the reduction of surface-wave power, especially in the E-plane [9−10]. As a result, the scanning range of a cavity-backed patch is larger than for a conventional antenna without cavity when used in a phased antenna array [11]. The cavity-backed design is also beneficial for heat dissipation [12], which may become an issue in future D-band phased antenna arrays due to significant amount of power dissipated on a small PCB area. The PCB vias can be used to spread the heat from the chip to the other side of the PCB.

Different types of cavity-backed antenna designs have been published for various applications. The early works on were done at frequencies below 30 GHz. In more recent publications, the frequencies range around 10-60 GHz [13]−[19]. For D-band frequencies (110−170 GHz), cavity-backed patch antenna arrays on PCB were presented in [7],[20],[21]. The 2×2 arrays were designed as a primary source for a lens or a transmitarray.

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The purpose of the cavity was the same as in this work, i.e. to suppress surface waves. However, in our work all the patches are surrounded by a cavity whereas the cavity is placed around the 2×2 arrays in [7],[20],[21]. In this work, all array elements are identical and can be multiplied to a larger array of any size.

In this paper, we present D-band patch antenna and 4×4 array designs on a cost-effective and low-loss multilayer build up which can be manufactured using PCB processing techniques. Semi-additive processing (mSAP) is used to reach the minimum required conductor width and spacing of 50 µm. The paper is organized as follows: PCB manufacturing process is described in Chapter II. In Chapter III, the designs of the D-band patch antenna element, the microstrip feed network, and the antenna array are presented. The S-parameter and radiation pattern measurements along with discussion are presented in Chapter IV.

II. PCB MANUFACTURING

The antennas in this work are designed on a 4-layer printed circuit board (PCB) shown in Fig. 1. The conductor layers 1−4 are denoted as L1−L4. Total thickness of the final PCB is 373µm including plated copper layers. Laser vias between thin and thick layers are sized 80 and 100 µm, respectively. Non-plated vias are available through the laminate. The waveguide probe designs used in testing require also dielectric material removal between layers L2−L4 which was accomplished with precision mechanical milling. Megtron 7N (ε_r = 3.20, tanδ = 0.003 at 50 GHz) by Panasonic [22] is chosen as substrate material because of its dielectric properties, dielectric thickness availability and ease of processing. Laminate and pre-preg materials are available down to 50-µm and 60-µm thicknesses.

The PCB was manufactured by using the high density interconnect (HDI) any-layer technology [22]. In the HDI PCB, all the electrical connections between the core and prepreg layers are done with laser-drilled microvias which are electroplated with copper. The HDI PCB enables smaller vias and catch pads, smaller line width and spacing, and a higher number of layers than the conventional PCB. The multilayer PCB is constructed by sequential lamination processing. In the standard commercial PCB production, the minimum line, spacing and laser drill diameter are 50/50/90 µm, respectively. In the advanced commercial production, the obtainable values are 40/40/75 µm [23].

A traditional method for PCB conductor patterning is the subtractive process, in which the copper layer is coated with an etch resist. Thereafter, photolithography is applied to image the areas where the copper should be retained, and then the un-imaged material is etched away [24]. The drawback is etching also in the horizontal direction, which reduces the accuracy of the conductor traces. As a result, the trace and gap widths are usually limited to about 75 µm at minimum [25]. For high frequency applications, accurate conductor patterning is required. At D-band frequencies a 100 µm pitch is needed for the (ground-signal-ground) GSG probes and flip-chip bumps which sets the maximum limit for the trace and gap widths to 50 µm. These requirements can be fulfilled by using semi-additive processing (mSAP) used in this work. In mSAP, a thin seed copper layer is coated onto the laminate and plated in the areas where the resist is not applied [24], [26]. Then the seed copper layer between conductors is etched away. The traces are formed with much greater accuracy having straight vertical shapes instead of trapezoidal ones of the subtractive process [24]. In the development work, the line and space widths even down to 15 µm have been reached by using the mSAP process [27].

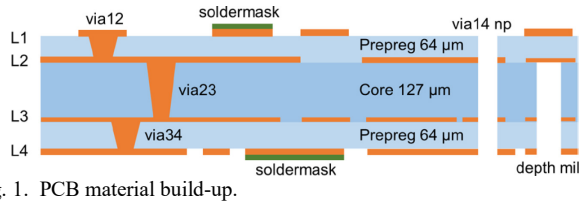

Fig. 1. PCB material build-up.

III. DESIGN

A. Antenna Element

The targeted operating frequency range for the antenna array is 140–160 GHz. The 20 GHz bandwidth around 150 GHz is about 14% and necessitates the use of wideband antenna elements. The cavity-backed aperture-coupled patch antenna (ACPA) is chosen as antenna topology. The ACPA enables independent optimization of the feed circuitry and the antenna operation. The ground plane isolates the feed line network and the active components from the radiators, and spurious radiation is reduced [28]. The cavity formed by vias is used to suppress surface waves.

The antenna is fed by using a microstrip line on layer L1 and the patch on layer L4 is excited though a coupling aperture in the ground plane on layer L2, see Figs. 1−2. The radiating patch is on the opposite side of the ground plane. Other end of the feeding microstrip line has a ground-signal-ground (GSG) pad configuration with 100-µm pitch to provide electrical interface for on-wafer probe measurements as well as for solder-bump integration with MMICs. The radiating patch is surrounded by vias and metal planes to suppress the substrate modes and hereby to increase broadside antenna gain. The antenna is designed and optimized using the Ansys HFSS full wave EM simulator.

A parametric analysis for the designed patch antenna by varying the main design parameters (l_p & w_p, l_{ap}, and l_{st}) is presented in Fig. 3. It can be observed that the center frequency is shifted from 137 GHz to 153 GHz when the patch size is decreased from 430 µm to 370 µm (Fig. 3(a)). The change in aperture length affects mostly on the $|S_{11}|$ level but also the center frequency and bandwidth (Fig. 3(b)). The matching stub length changes the $|S_{11}|$ level and bandwidth (Fig. 3(c)). The choice for the final values for the antenna test structures is based on an appropriate center frequency of 142 GHz and an adequate bandwidth and $|S_{11}|$ level.

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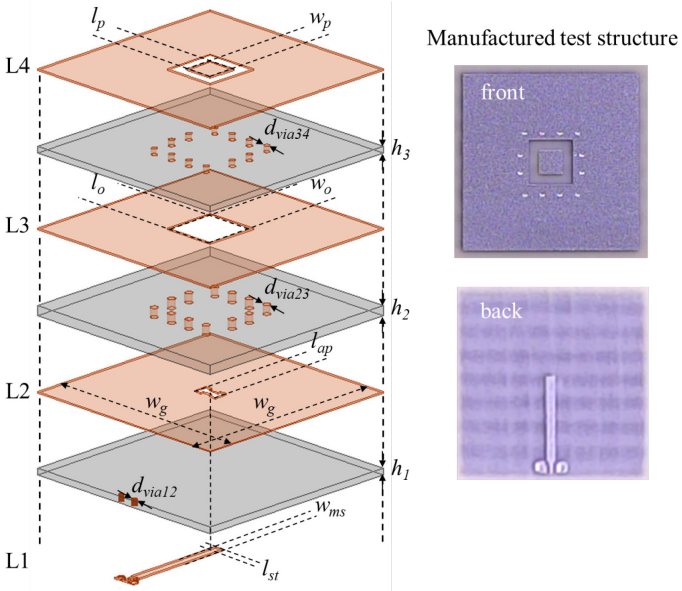

Fig. 2. D-band aperture-coupled patch antenna design. The patch dimensions are l_p= w_p =410µm. The ground openings are l_o= w_o =750µm and l_{ap}=350µm. Microstrip line width is w_{ms}=140µm. The matching stub length is l_{st}=150µm. Via diameters are d_{via12}= d_{via34}=80µm and d_{via23}=100µm. Substrate thicknesses are h_1= h_3 =64µm and h_2 =127µm.

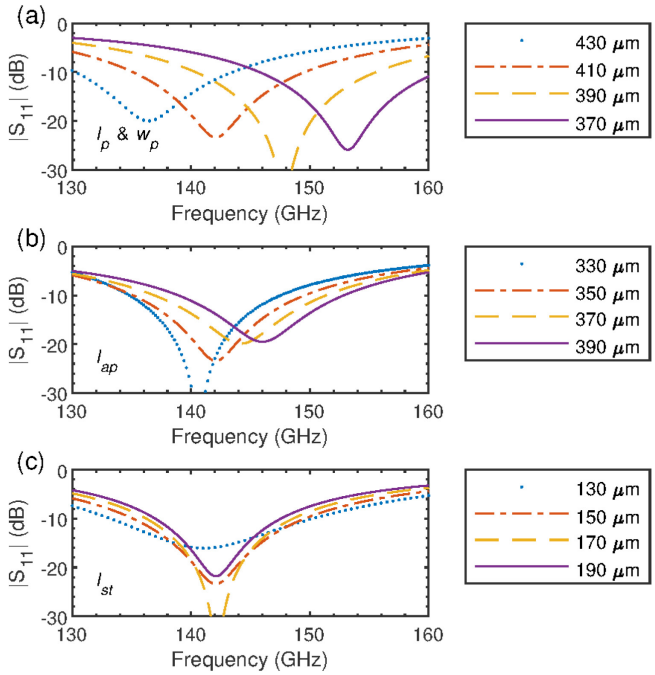

Fig. 3. Parametric analysis for the patch antenna with variation of the main design parameters: (a) size of the patch (l_p and w_p), (b) coupling aperture length (l_{ap}), and (c) matching stub length (l_{st}).

The final antenna dimensions are shown in Fig. 2 and in Table I. Test structures are also designed for studying the coupling between the designed antennas when placed in antenna arrays. Those include two antennas having 1 mm (λ_0/2 at 150 GHz) separation arranged in E-plane, H-plane, or E/H-plane configuration.

TABLE I
D-BAND PATCH ANTENNA ELEMENT DIMENSIONS

Parameter	Description	Value
d_{via12}	via L1-L2 diameter	80µm
d_{via23}	via L2-L3 diameter	100µm
d_{via34}	via L3-L4 diameter	80µm
h_1	dielectric L1-L2 thickness	64µm
h_2	dielectric L2-L3 thickness	127µm
h_3	dielectric L3-L4 thickness	64µm
l_{ap}	coupling aperture length	350µm
l_o=w_o	ground opening size	750µm
l_p=w_p	patch size	410µm
l_{st}	matching stub length	150µm
w_{ms}	microstrip line width	140µm

B. Antenna Array

A 16-element planar antenna array is designed to demonstrate feasibility of the patch antenna in an array configuration. The element separation is 1 mm (λ_0/2) which will enable maximum scanning range in a phased array under development. The total size of the array is 4.25 mm × 4.25 mm. A single feeding line is needed for the RF testing of the array test structure. Thus, a microstrip-line feeding network from 1 input to 16 outputs is designed. The requirements for the feed network are good input and output return loss and the same amplitude and phase for all array ports. The corporate feed network consists of quarter-wave matched T-junctions and 50-Ω matched microstrip lines (width 140 µm), see Fig. 4.

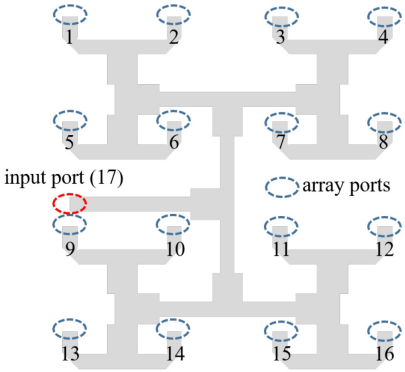

Fig. 4. Feed network for the 16-element patch antenna array.

The feed network is optimized for 140−160 GHz using AWR Microwave Office circuit simulator. The final layout is simulated using the AWR Axiem electromagnetic (EM) tool based on the Method of Moments (MoM). The EM simulated input return loss (RL) is better than 10 dB above 135 GHz, at least up to 170 GHz. The output RLs are between 7 dB and 9 dB around the center frequency of 143 GHz. The output RLs are lower than the input RL due to the inherent characteristics of the reactive T-junction power dividers. In the circuit simulation, the insertion loss (IL) for any output is 12.3−12.5 dB (ideally 12 dB) above 140 GHz. In the EM simulation results, the IL varies between 12 dB and 15 dB at around 143 GHz. The variation is due to non-identical microstrip paths in the actual geometry of the feed network. The insertion phase difference is within 15° at 145 GHz. The differences in the IL

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cause uneven amplitudes in the array elements. In a phased array under development, each array element has an amplifier and a phase shifter and possible amplitude and/or phase imbalance of the feed network can be compensated on an integrated circuit (IC). The complete array including the feed network is simulated using the Ansys HFSS EM simulator. The simulation model and the micrographs of the manufactured array structures are shown in Fig. 5.

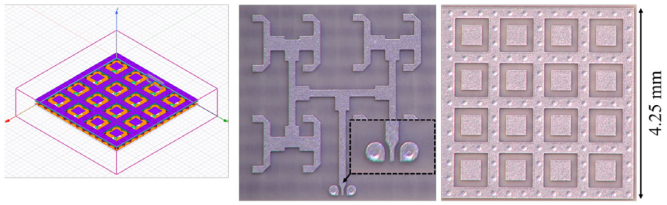

Fig. 5. 16-element antenna array. (a) simulation model and micrographs of the (b) feed network side and (c) patches side of the manufactured prototype.

IV. Results and Discussion

The transmission line, antenna element, and antenna array test structures were manufactured with semi-additive processing (mSAP) for conductor patterning. The micrographs of the manufactured antenna and array structures shown in Figs. 2 and 5 clearly exhibit the very good manufacturing accuracy, in particular, observable in the GSG area. The realized patch dimensions are only about 10 µm (2.5%) smaller than the designed ones. The S-parameters were measured on a probe station. The stand-alone feed network was not characterized due to lack of 50-Ω terminations for the array ports when measuring with a 2-port vector network analyzer (VNA). Radiation patterns of the antenna element and the array were measured using a near-field scanner as will be later described.

A. S-parameters

The S-parameters of the antenna element, antenna array, and transmission lines were measured at D-band (110–170 GHz) using PNA-X N5245A with WR6.5-VNAX extenders and GSG probes with 100-µm pitch. A Rohacell foam slab and an RF absorber were placed below the antenna-under-test (AUT) to emulate far-field radiation conditions. The simulated and measured $|S_{11}|$ for a single antenna are presented in Fig. 6. The thru-reflect-line (TRL) calibration method is used in the measurements, thus the GSG transition needed for the probes is extracted from the results. The simulated and measured $|S_{11}|$ are below -10 dB at 135−149 GHz and 138−158 GHz, respectively. Good correlation between the simulation and the measurement can be observed. The higher measured center frequency is due to about 10 µm (2.5%) smaller realized patches than the designed ones.

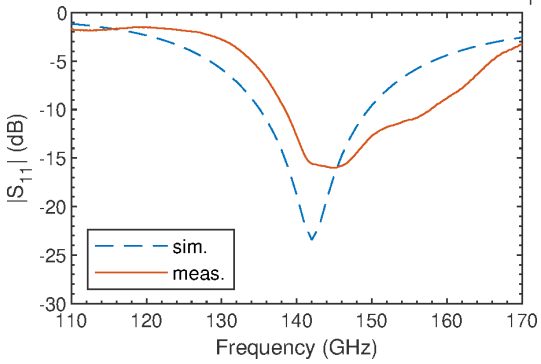

Fig. 6. Simulated and measured $|S_{11}|$ of the antenna element.

The measurement results for antenna coupling test structures including two antennas having 1 mm ($\lambda_0/2$) separation arranged in E-plane, H-plane, or E/H-plane configuration are shown in Fig. 7. The coupling between two antennas is between -17 and -20 dB in the E- and H-planes around the antenna center frequencies, see Fig. 7, which is still acceptable for array elements. In the E/H-plane configuration, the coupling is below -40 dB.

The simulated and measured $|S_{11}|$ for the array are shown in Fig. 8. The array is well matched into 50 Ω around 143 GHz and the measured $|S_{11}|$ is below -10 dB at 135−155 GHz. Fig. 9 shows the measured insertion loss of 1.9 dB/cm and 1.8 dB/cm for microstrip line (MS) and grounded coplanar waveguide (GCPW), respectively, at 150 GHz. Such small transmission line losses enable the construction of feed networks even for larger antenna arrays in the future, such as 64-, 256- or 512-elements.

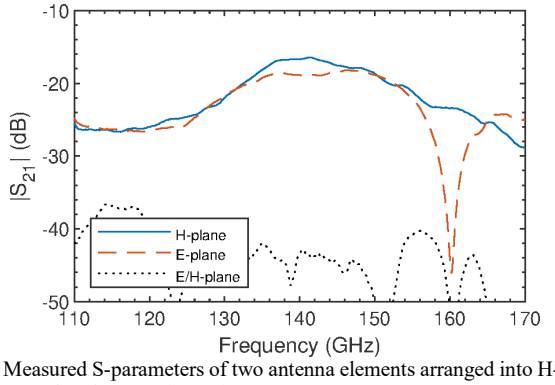

Fig. 7. Measured S-parameters of two antenna elements arranged into H-plane, E-plane, or E/H-plane configuration.

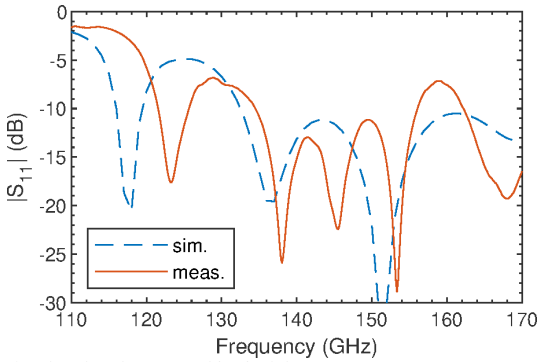

Fig. 8. Simulated and measured $|S_{11}|$ of the antenna array.

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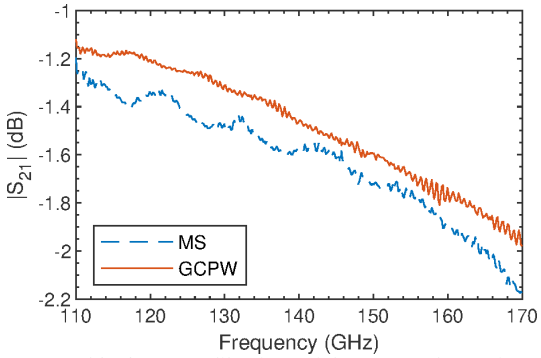

Fig. 9. Measured $|S_{21}|$ (TRL calibration) of the 9.1 mm long microstrip line (MS) and grounded coplanar waveguide (GCPW) on PCB. The $|S_{11}|$ is below -18 dB (MS) and below -25 dB (GCPW) at 110−170 GHz. The line losses for MS and GCPW are 1.9 dB/cm and 1.8 dB/cm, respectively, at 150 GHz.

The effect of surface roughness on the conductor losses was analysed for a microstrip line. First, surface profiles of PCB conductor surfaces were measured by using an optical profilometer. Based on the measured profiles, a root-mean-square (RMS) surface roughness was determined. The surface roughness (*sr*) varied between 240 nm and 430 nm (see Fig. 10). Thereafter, the 9.1 mm long microstrip line was simulated in Ansys HFSS 3D electromagnetic (EM) solver by varying the RMS surface roughness parameter from 0 nm to 400 nm in the Groisse model [29]. The simulations and the measurement are compared in Fig. 11. For an ideally smooth conductor, i.e., for *sr* = 0 nm, the insertion loss (IL) is 0.95−1.2 dB at 110−170 GHz. The insertion loss increases with increasing *sr*. For *sr* = 400 nm, the IL is 1.35−1.75 dB. The measured IL is close to the simulation with *sr* = 400 nm up to 145 GHz. At higher frequencies the measured IL is higher. The higher loss could be due to the fact that the conductors have a higher roughness on the dielectric side than on the top side to improve adhesion [30], which may have a stronger impact on the losses at high frequencies. Unfortunately, accurate data for the dielectric side roughness was neither available nor possible to be measured for the test structures. The measured IL is 1.25−2.2 dB at 110−170 GHz. At 150 GHz, the difference between the measured line and the simulated ideally smooth line is 0.7 dB, i.e., 0.77 dB/cm.

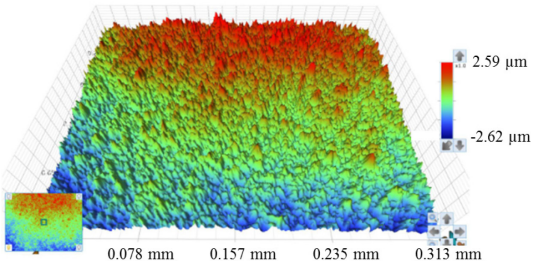

Fig. 10. Surface roughness of the PCB conductors measured by using an optical profilometer. The RMS roughness in the picture is 350 nm.

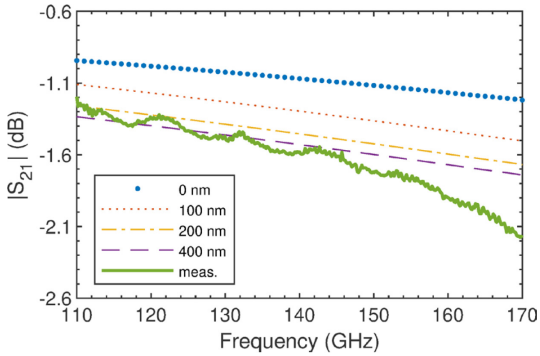

Fig. 11. Simulated and measured insertion loss of a microstrip line with different surface roughness values in simulation.

B. Radiation patterns

The radiation patterns of the antennas were determined with the planar near-field measurement, see Fig. 12 for the measurement set-up. A custom WR-6 waveguide fixture was designed and fabricated for the radiation pattern measurements to provide a transition from a WR-6 waveguide to a microstrip feed line of the AUT, named as wg-to-ms transition in Fig. 12. Two separate back-to-back transitions were manufactured and tested to determine the losses of the fixture. The measured insertion loss was around 8 dB at 120–145 GHz and increased at higher frequencies. Based on two separate measurements of the two test structures, it was observed that the results were identical up to 155 GHz but had variations of up to 2−3 dB at higher frequencies. The reason for the variations could be the realized non-perfect milling of the PCBs and resulting variation in the alignment of the PCBs inside the transitions. The transition loss was taken into account when determining the measured antenna gain of the test structures. Due to transition loss variations, the antenna gain could be reliably determined up to 155 GHz because of the limited calibration.

Antenna aperture filtering process was utilised to avoid the effects of the reflections from the support structures and the observed small radiation leakage from the waveguide flange in the measured radiation patterns. Fig. 13 shows the flow-chart describing the near-field measurement and the following antenna aperture filtering process. First, the near-field was sampled at the distance d = 26 mm from the antenna using an open-ended WR-5 waveguide as the probe antenna. Then, the near-field was back-propagated to the antenna plane (z = 0) using the plane wave spectrum decompositions. The obtained field at the antenna plane was filtered, i.e., the field outside the selected apertures of 6.7 mm × 6.7 mm and 11.8 mm × 11.8 mm

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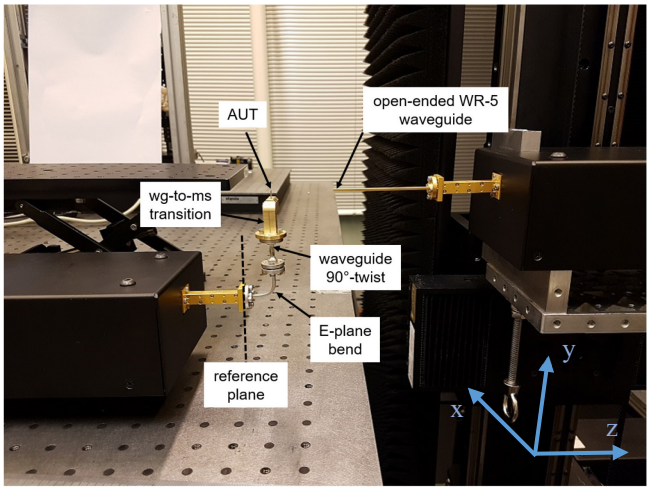

Fig. 12. Near-field measurement set-up. Open-ended WR-5 waveguide probe is attached to the VNA mm-wave extension, which is on the carriage of the planar near-field scanner. The probe is moved in the *xy*-plane to sample the near field. The absorbers are removed for clarity.

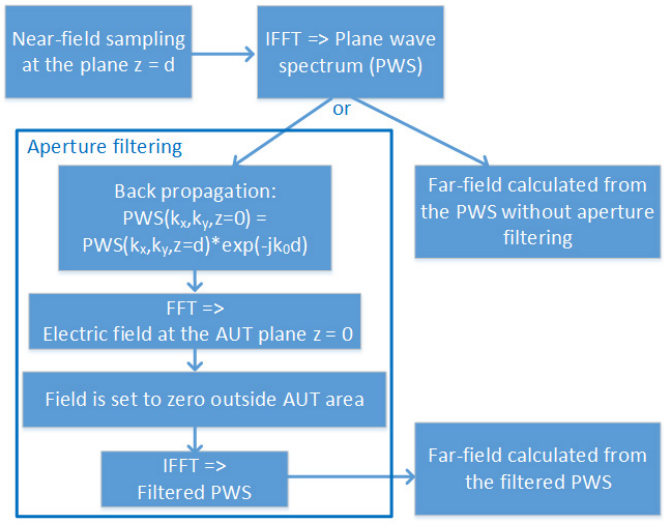

Fig. 13. Flow-chart for the near-field measurement and the antenna aperture filtering process.

for the patch and antenna array, respectively, was set as zero. Finally, the radiation patterns were calculated using the normal far-field calculation from the plane wave spectrum data.

For the antenna gain measurements, a horn antenna was used as a reference, the reference point being the waveguide output of the frequency extension unit. Therefore, the compensation of the losses in the waveguide components before the feeding point of the antenna-under-test (AUT) had to be made. The components and the corresponding compensated losses included: waveguide 90°-twist having 0.45 dB loss (measured), E-plane bend having 0.6 dB loss (measured), and waveguide to microstrip transition, including an 11.7-mm long feeding microstrip line. The measured transition loss is varying from 4 dB to 7.5±1.5 dB in the frequency range of 130 GHz to 170 GHz.

Figs. 14 and 15 show the azimuth and elevation patterns of the measured realized gain at 132 GHz, 143 GHz, and 155 GHz for the patch antenna element and the 16-element array, respectively. The agreement between the measured and

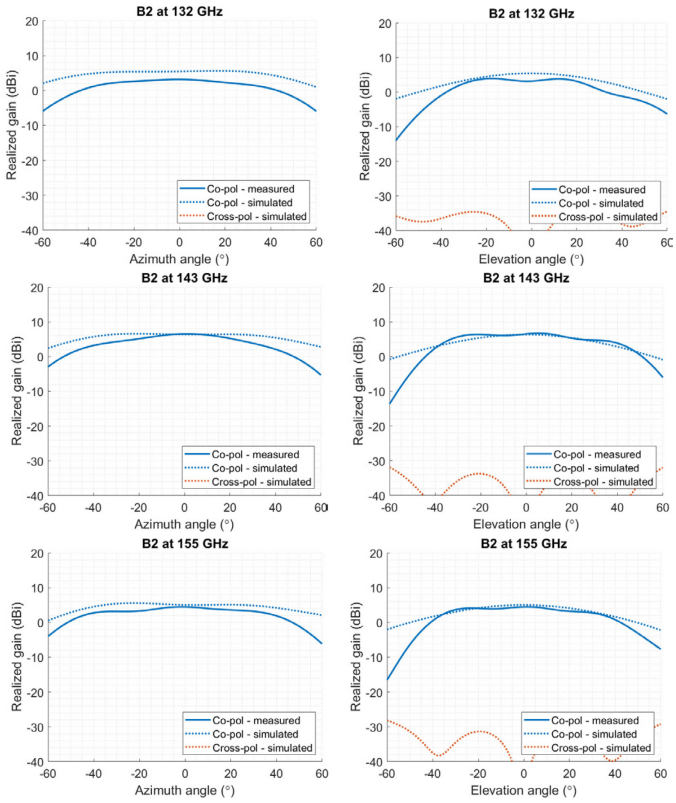

Figure 14. Measured and simulated realized gain patterns of the patch antenna element at 132, 143, and 155 GHz. Azimuth cuts are on the left and elevation cuts are on the right. Measured cross-polarization patterns are not available. Note, that simulated cross-polar patterns are below −40 dBi in the azimuth cuts because of the antenna symmetry in this plane.

simulated patterns is good for the co-polarized case, the best agreement being at 143 GHz for the array. For the individual patch element, the agreement collapses for the elevation cut at the large angles. This might be caused by the limited scan area in the near-field measurement. The so-called valid angle is 60° and the measurement accuracy is affected already at smaller angles. However, the agreement is much better in the azimuth plane and the measured peak gain level is very well in accordance with the simulated one.

The simulated cross-polarization is low, well below −30 dBi, in the principal planes for the patch antenna. For the azimuth, i.e., symmetry plane, the cross-polarization level is even lower. Unfortunately, only co-polarization measurement results are available for the patch. The measured cross-polarization of the array is below −10 dBi, and the level is well in line with the simulated results, although there are deviations in the patterns. The orientation of the array may have been slightly tilted in the measurement setup, which increases the measured cross-polarization level.

The effect of surface roughness on the antenna array gain was simulated with the roughness value of sr = 400 nm in the Groisse model for the conductors. The gain was 0.7 dB lower than with ideally smooth conductors. Thus, the surface roughness of the PCB conductors do not have a major impact on the array performance even at D-band frequencies.

Fig. 16 shows the measured and simulated gain curves and the simulated directivity over the frequency for the patch and

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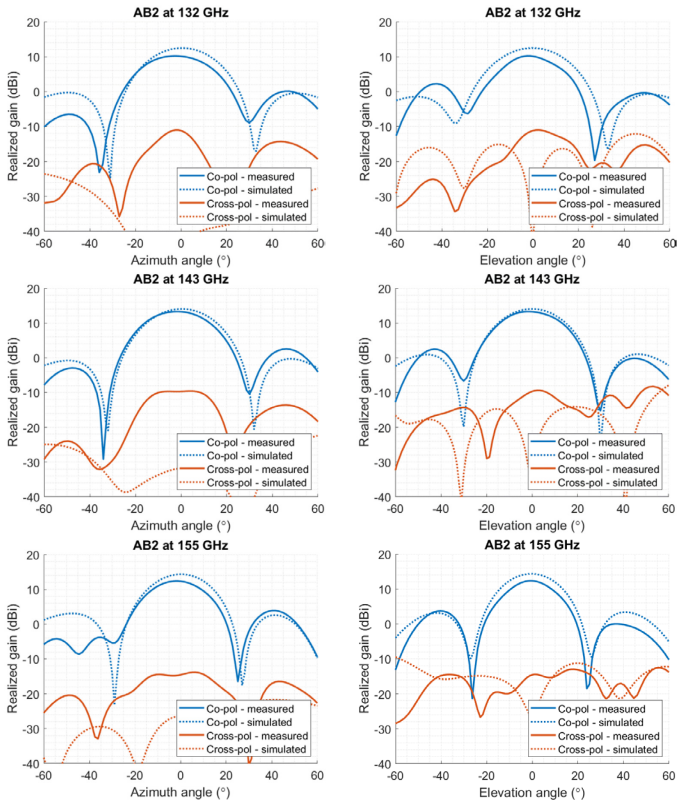

Figure 15. Measured and simulated realized gain patterns of the patch antenna arrays at 132, 143, and 155 GHz. Azimuth cuts are on the left and elevation cuts are on the right.

antenna array. The radiation pattern and gain measurements were conducted using nominally 140–220 GHz vector network analyzer extension units and, thus, the frequency range of the gain measurements is limited at the lower end of the frequency range. The agreement between the simulation and measurement results is reasonable. For the array, the measured gain is approximately 1 dB less than the simulated one with the maximum of 14 dBi at 143 GHz. For the patch antenna, the agreement is similar, and the measured maximum gain is 7 dBi at 143 GHz. The measured gain curves are limited up to 155 GHz due to uncertainty of the transition loss for higher frequencies. It is not possible to measure the efficiency of the low gain antennas accurately with the planar near-field measurement technique because of the limited angular range of the measurement setup. The antenna efficiency can be

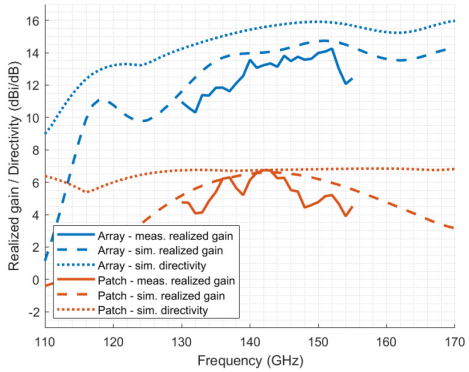

Fig. 16. Measured and simulated realized gain and the simulated directivity with respect to the frequency.

TABLE II
COMPARISON OF D-BAND ANTENNA DESIGNS

	[7],[21]	[8]	[20]	This work
Freq. (GHz)	114-138	136-157	110-140	135-155
Techn.	PCB	LCP	PCB	PCB
ε_r	2.94/3.52	2.9	3.4	3.2
$\tan\delta$	0.0012/0.004	0.0025	0.005	0.003
Type	2×2 PA*	GAA**	2×2 PA*	4×4 PA***
Gain (dBi)	8.4	14.5	7.8	14
BW	19%	14%	20%	14%

*PA = cavity-backed patch antenna array, primary source for transmitarray or lens
**GAA = grid array antenna
***PA = stand-alone cavity-backed patch antenna array

estimated as a relation between the measured antenna gain and the simulated directivity. The difference between the gain and directivity for the patch is about 0.2 dB at minimum being below 1.5 dB in the frequency range of 132−157 GHz. For the antenna array, the difference is about 1.5 dB at the operation frequency giving about 71% as the antenna efficiency.

A comparison of the proposed D-band antenna design with published solutions is shown in Table II. The bandwidth and gain of the 4×4 array are quite similar to the ones in [8] for the grid array antenna. Here, the array gain is higher than in [7],[20],[21] obviously due to higher number of elements. But, since the single-element gain here is about 7 dBi, it can be assumed that the gain of 2×2 arrays would also exceed the ones presented in [7],[20],[21]. The main advantage of the proposed antenna design is the scalability for the future phased antenna arrays due to the isolated antenna elements.

V. CONCLUSIONS

Design, manufacturing considerations and characterization of a D-band patch antenna and an array on a multilayer high-frequency PCB were presented in this paper. The feasibility of PCB technology for a low-cost integration platform even at D-band is proven. The presented D-band antennas and PCB substrate technology show good performance and enable the integration of complex MMICs and antennas into scalable phased antenna arrays.

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