D-band SiGe BiCMOS Power Amplifier with 16.8dBm P_{1dB} and 17.1 % PAE Enhanced by Current-Clamping in Multiple Common-Base Stages

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***Abstract*—This letter presents single-ended and differential D-band power amplifiers (PAs) in 55nm SiGe BiCMOS technology. The proposed PAs exploit the remarkable features of common-base stages for rising the power efficiency, i.e. (1) higher breakdown voltage, (2) sharp compression profile thanks to the enhanced linearity and (3) supply current adapted to the signal amplitude by means of current clamping. A 4-stage single-ended PA proves P_{1dB} = 16.8 dBm with P_{SAT} = 17.6 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB\text{-}6dB}$ are 17.1 % and 8.5 % respectively. With a differential PA the linear output power is increased to P_{1dB} = 18.5 dBm with P_{SAT} = 19.3 dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB\text{-}6dB}$ are 12.6 % and 6.7 % respectively. The PAs demonstrate 3× PAE improvement in the linear region against state of the art.**

***Index Terms*—Amplifier, BiCMOS integrated circuits, Common base, D-band, millimeter wave integrated circuits, Power amplifier.**

I. Introduction

THE never ending demand for wider bandwidth, coupled with the evolution of technology, drives the progress of silicon ICs beyond 100 GHz. The D-band, 60 GHz centered at 140 GHz, is being considered for enhanced resolution radars and wireless transceivers with a fiber-like transport capacity, key for network deployment in 5G and beyond [1]. The power amplifier (PA) is an essential component in such systems.

D-band PAs in silicon (both SiGe HBTs and CMOS) demonstrated a saturated output power (P_{SAT})≥14 dBm [2]–[7]. PAs reported so far are implemented by cascading multiple Class-A common-emitter (source) or cascode stages. Due to soft saturation, the output power at 1 dB gain compression (P_{1dB}) is remarkably lower than P_{SAT}, where the efficiency peaks, and PAE drops very sharply when $P_{out} \leq P_{1dB}$ [2]–[7]. Considering the peak-to-average power ratio of typical QAM modulations, PAs are operated at 5-8 dB back-off from P_{1dB} where the PAE of reported PAs is 2% or less [2]–[7]. The maximum available gain (MAG) of transistors in D-band is only of few dBs. This issue limits the design options and techniques for back-off PAE improvement like Doherty PAs or even simple Class-AB biasing are not viable.

This work proposes D-band PAs leveraging the remarkable features of common-base (CB) stages to enhance PAE. Compared to common-emitter (CE), the CB enjoys the following advantages: (1) extended breakdown, thus higher usable supply voltage, (2) linearity enhanced by the emitter degeneration impedance, leading to a sharp compression with P_{1dB} close to P_{SAT}, (3) supply current adapted to the signal amplitude by current-clamping [8], with transistors nearly in Class-A, thus raising the PAE in back-off with negligible gain penalty. To the Author's best knowledge this is the first time the advantages of CB stages are fully exploited for D-band PAs. The realized PAs, in 55nm BiCMOS technology, achieve a state-of-the-art output power with 3× or more higher PAE at P_{1dB} and at 6-dB back-off.

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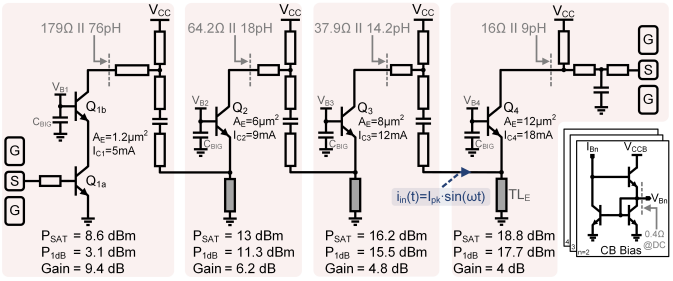

Fig. 1: Schematic of the single-ended PA.

II. Circuit Design

The schematic of the single-ended (s.e.) PA, comprising four stages, is drawn in Fig. 1. The transistor in the output stage, Q_4, is composed of 2 parallel HBTs each with emitter area of $A_E = 6\,\mu m^2$. Considering the breakdown voltage $BV_{CB0} = 5$ V,

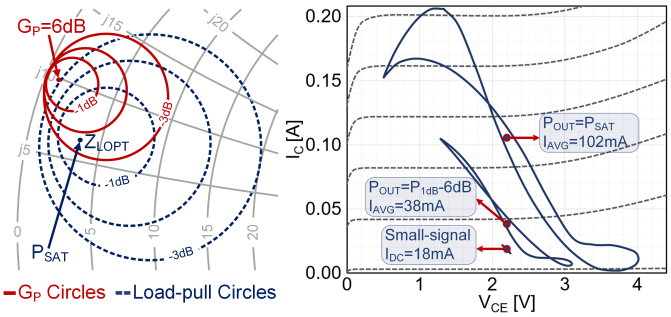

Fig. 2: G_P and load-pull circles and dynamic load lines for the transistor in the output stage.

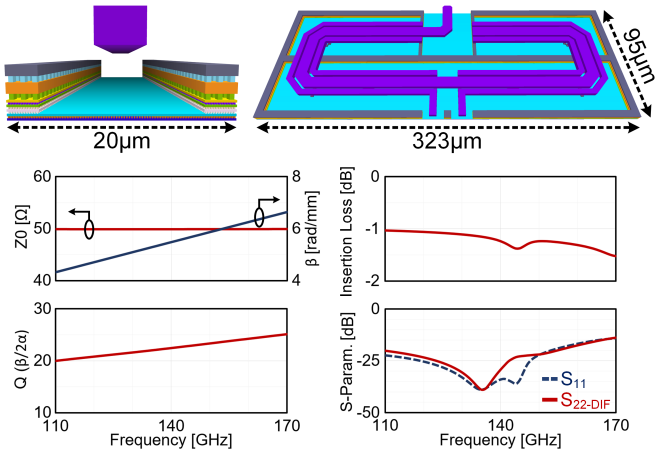

Fig. 3: Characteristics of T-Line and balun.

a supply voltage $V_{CC} = 2.2\,V$ is selected. From load-pull simulations, drawn in Fig. 2, the load impedance for maximum output power is $Z_{L-opt} = 3.51 + j{\cdot}6.62\ (16\,\Omega\,//\,9\,pH)$ and, including the loss of the output matching network, the device delivers $P_{1dB} = 17.7\,dBm$, very close to $P_{SAT} = 18.8\,dBm$. If a cascode configuration is formed with the same transistor under the same supply, $P_{SAT} = 15.2\,dBm$ with a substantially lower $P_{1dB} = 11.7\,dBm$. Still, with the transistor in CE configuration the supply voltage must to be reduced (being $BV_{CE0} = 1.5\,V$) leading to $P_{1dB} = 8.9\,dBm$ only.

Notice that from the DC viewpoint Q_4 is in CE configuration. To withstand 2.2 V supply the base voltage is set by a Wilson current mirror (drawn in Fig. 1) which shows a very low impedance ($< 1\Omega$). In this way impact-ionization generated holes by the collector DC voltage can flow out of the base of Q_4, rising the breakdown sufficiently above BV_{CE0} [9].

To improve the power efficiency, the quiescent current is set low, $I_{Q4} = 18\,mA$, and current clamping is leveraged to adapt the supply current to the signal amplitude. If the current flowing into the emitter of Q_4, $i_{in}(t) = I_{pk}\sin(\omega t)$, exceeds I_{Q4} the BE junction turns off for a small fraction of the period

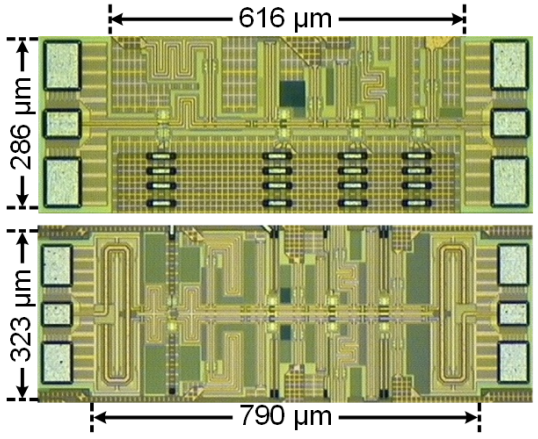

Fig. 4: Chip microphotographs of the single-ended (top) and differential (bottom) PAs.

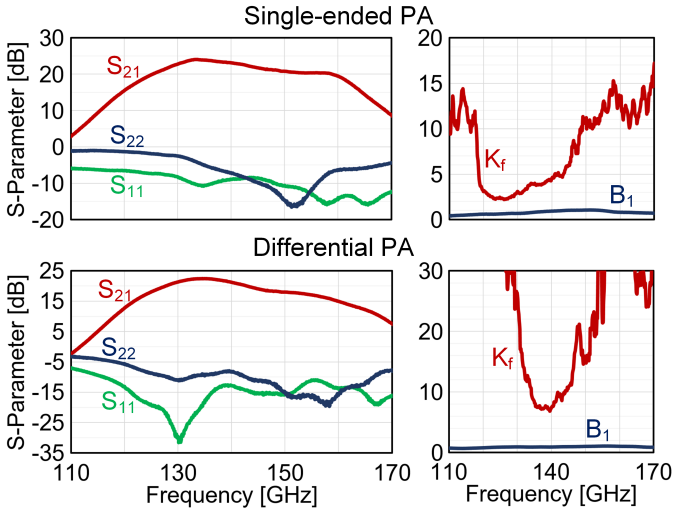

Fig. 5: Measured S-parameters and stability-factors for single-ended and differential PAs.

and $i_{in}(t)$ charges the transmission line stub from the emitter of Q_4 to ground (TL_E), which works as an inductor. Q_4 then turns on with an average current raised roughly to I_{pk}. The effectiveness of supply current modulation performed by Q_4 is evidenced by the dynamic load-lines plotted in Fig. 2 on top of the device I-V curves. At small P_{out} the collector current of Q_4 swings around the quiescent point. But when P_{out} rises, the average current increases and the load-line is shifted upward. Looking at the load-pull contours in Fig. 2 the selected Z_{L-opt} sacrifices 2 dB of power gain (G_P). Adding the losses of the matching network (∼1 dB) and GSG pad (∼0.5 dB), the output stage displays $G_P = 4\,dB$ only (it is worth noticing that the same device in CE features $G_P = 2.5\,dB$, lower than CB [10]). The low G_P of the last PA stage makes the preceding stages critical for the overall performances. They have to rise gain while delivering enough power to push the last stage into compression without penalizing P_{1dB} of the complete amplifier. To meet this target CB transistors (Q_2 and Q_3 in Fig. 1) are still selected for the two middle stages, delivering high power with a sharp compression and allowing to exploit current clamping for efficiency improvement. The average current rising proportionally to the signal leads also to a mild (0.5 dB) gain expansion in each stage, useful to flatten the overall gain profile and maintain P_{1dB} close to P_{SAT}. Device sizes are scaled down at constant current density and the matching networks are designed favoring gradually power gain to the peak power. An input stage is finally added to rise the total power gain above 20 dB. The cascode configuration, featuring high G_P, is selected ($Q_{1a} - Q_{1b}$ in Fig. 1) with transistors biased in Class-A at ∼5 mA constant current.

Matching networks are realized with transmission lines (Tlines) and MOM capacitors. The cross section and the simulated performance of Tlines, customized for small footprint (20 µm width) and low loss (Q≈23), are reported in Fig. 3. A differential PA has been also implemented, by using two instances of the s.e. design with Marchand baluns (shown in Fig. 3) introducing ∼1.1 dB simulated insertion loss.

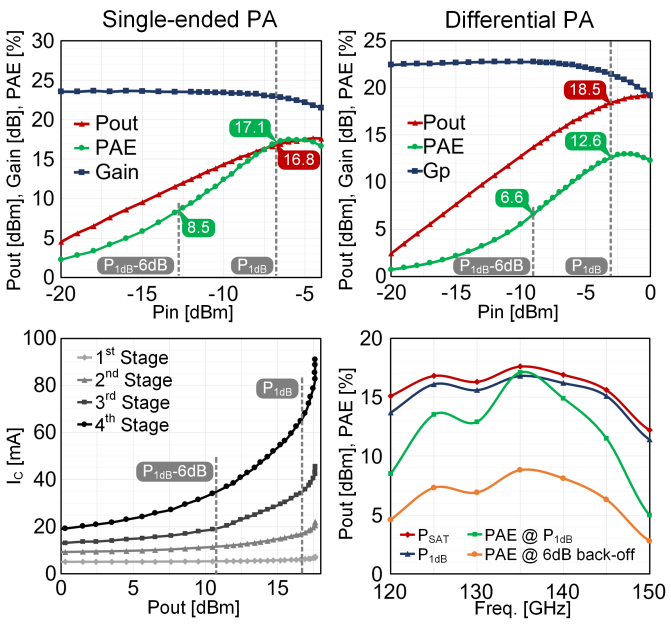

Fig. 6: Measured large signal performance.

TABLE I: Performance summary and comparison to prior works.

Ref	This Work		[2]	[3]	[4]	[5]	[6]	[7]
Tech.	55nm SiGe		90nm SiGe	130nm SiGe	120nm SiGe	130nm SiGe	16nm FinFET	40nm CMOS
Supply [V]	2.2		1.6	1.5, 3.3	3.5	4	1	1
Freq. [GHz]	135		116	130	120	160	135	140
Gain [dB]	24	22.4	15	28.5	32	27	20.5	20.3
S_{21}-BW [GHz]	34	25	15	16	17.2	50	22	17
P_{SAT} [dBm]	17.6	19.3	20.8	15*	17.8	14	15	14.8
P_{1dB} [dBm]	16.8	18.5	17	12.6*	13.5	11.8	9.2	10.7
PAE_{MAX} [%]	17.5	13	7.6	8.2*	4.3	5.7	12.8	8.9
PAE@P_{1dB} [%]	17.1	12.6	4	5.8*	-	2.5	4.5*	4*
PAE @6dB backoff	8.5	6.7	1.2*	2.2*	-	<1*	1.2*	<1*
FoM	37.5	28.3	0.9	12.6	-	4.9	0.8	1.0

*: estimated from measurement plots

$FoM = 10^{-3} \cdot P_{out} \cdot G \cdot PAE \cdot f^2$ [12]

III. Experimental Results

The single-ended and differential amplifiers were fabricated in STMicroelectronics' 55 nm SiGe technology [11] with a 0.18 mm^2 and 0.26 mm^2 silicon area respectively. Fig. 4 shows the chip microphotograps.

From the small-signal measurements in Fig. 5 the PAs are unconditionally stable. The s.e. design reaches $S_{21} > 20$ dB from 125 GHz to 159 GHz with $S_{21-max} = 24$ dB at 133 GHz. The differential PA shows $S_{21} > 18$ dB from 125 GHz to 150 GHz with $S_{21-max} = 22.4$ dB at 135 GHz.

Large signal measurements are reported in Fig. 6. The s.e. PA displays $P_{SAT} = 17.6$ dBm and $P_{1dB} = 16.8$ dBm at 135 GHz. The PAE at P_{1dB} is 17.1 % and still 9.5 % at $P_{1dB-6dB}$. At 135 GHz the differential PA exhibits $P_{SAT} = 19.3$ dBm and $P_{1dB} = 18.5$ dBm. The PAE at P_{1dB} and $P_{1dB-6dB}$ is 12.6 % and 6.7 %. As shown by the bottom-left plot, the measured DC current drawn by CB stages in the s.e. PA rises with P_{out} up to 5 times the quiescent value thanks to current-clamping. The total DC current at P_{1dB} is ~130 mA, and it is nearly one-half at $P_{1dB-6dB}$, leading to a Class-B like back-off PAE profile. From the bottom-right plot, reporting P_{out} and PAE of the s.e. PA over frequency, $P_{1dB} \geq 15$ dBm with PAE $\geq$ 11% at P_{1dB} and >6% at 6 dB back-off from 125 GHz to 145 GHz. In the differential PA (measurements are not shown), $P_{1dB} > 17$ dBm with PAE $\geq$ 9% at P_{1dB} and >5% at 6 dB back-off from 125 GHz to 140 GHz.

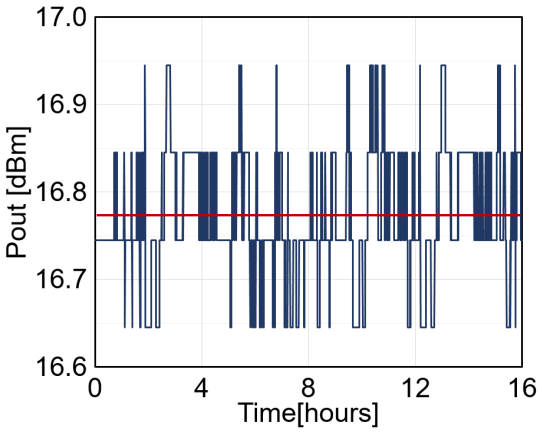

Fig. 7: Reliability test for single-ended PA.

The single ended PA driven at P_{1dB} has been tested with 16-hour continuous operation showing ±0.15 dB variation around P_{out} of 16.8 dBm. The result of measurement is plotted in Fig. 7.

The best measured performances are compared with silicon PAs at similar frequency delivering $P_{SAT} > 14$ dBm in Table 1. P_{1dB} is aligned with [1] but from 3 to 6 dB higher than [2]-[7]. The efficiency at P_{1dB} and in power back-off is improved by 3× or more over state of the art. The PAs performances are compared also with the Figure of Merit (FoM) introduced in [12] (with expression reported as foot note in Table I). The FoM, calculated at P_{1dB}, confirms the remarkable improvement against state of the art.

IV. Conclusion

D-Band power amplifiers in 55nm SiGe BiCMOS technology have been presented. The PAs exploit the remarkable features of common-base stages to enhance power-added-efficiency in the linear PA operating region. A single-ended PA proves $P_{1dB} = 16.8$ dBm with $P_{SAT} = 17.6$ dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ are 17.1 % and 8.5 % respectively. With a differential PA the linear output power is increased to $P_{1dB} = 18.5$ dBm with $P_{SAT} = 19.3$ dBm at 135 GHz. The PAE at P_{1dB} and at $P_{1dB-6dB}$ are 12.6 % and 6.7 % respectively, an improvement of at least 3× against state of the art.

REFERENCES

[1] M. G. L. Frecassetti, A. Mazzanti, J. F. Sevillano, D. del Río and V. Ermolov, "D-Band Transport Solution to 5G and Beyond 5G Cellular Networks," 2019 European Conference on Networks and Communications (EuCNC), Valencia, Spain, 2019, pp. 214-218.

[2] H. Lin and G. M. Rebeiz, "A 110-134-GHz SiGe Amplifier With Peak Output Power of 100-120 mW," IEEE TMTT, vol.62, no.12, pp.2990-3000, Dec.2014.

[3] A. Visweswaran et al., "A 112-142GHz Power Amplifier with Regenerative Reactive Feedback achieving 17dBm peak Psat at 13% PAE," IEEE ESSCIRC 2019, pp.337-340..

[4] R. B. Yishay and D. Elad, "A 17.8dBm 110-130 GHz Power Amplifier and doubler chain in SiGe BiCMOS technology," 2015 IEEE RFIC, pp.391-394.

[5] M. Furqan, F. Ahmed, B. Heinemann and A. Stelzer, "A 15.5-dBm 160-GHz High-Gain Power Amplifier in SiGe BiCMOS Technology," in IEEE Microwave and Wireless Components Letters, vol. 27, no. 2, pp. 177-179, Feb. 2017, doi: 10.1109/LMWC.2016.2646910.

[6] B. Philippe and P. Reynaert, "24.7 A 15dBm 12.8%-PAE Compact D-Band Power Amplifier with Two-Way Power Combining in 16nm FinFET CMOS," 2020 IEEE ISSCC, pp.374-376.

[7] D. Simic and P. Reynaert, "A 14.8dBm 20.3dB Power Amplifier for D-band Applications in 40nm CMOS," 2018 IEEE RFIC, pp.232-235.

[8] E. Rahimi et al., "High-Efficiency SiGe-BiCMOS E-Band Power Amplifiers Exploiting Current Clamping in the Common-Base Stage," IEEE JSSC, vol.54, no.8, pp.2175-2185, Aug.2019.

[9] M. Rickelt, H. M. Rein and E. Rose, "Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors," in IEEE Transactions on Electron Devices, vol. 48, no. 4, pp. 774-783, April 2001, doi: 10.1109/16.915725.

[10] Z. Ma and N. Jiang, "On the operation configuration of SiGe HBTs based on power gain analysis," in IEEE Trans. on Electron Devices, vol.52, no.2, pp.248-255, Feb.2005.

[11] P. Chevalier et al., "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz fT / 370 GHz fMAX HBT and high-Q millimeter-wave passives," 2014 IEEE International Electron Devices Meeting, San Francisco, CA, 2014, pp. 3.9.1-3.9.3, doi: 10.1109/IEDM.2014.7046978.

[12] R. Brederlow, W. Weber, J. Sauerer, S. Donnay, P. Wambacq and M. Vertregt, "A mixed-signal design roadmap," in IEEE Design & Test of Computers, vol. 18, no. 6, pp. 34-46, Nov.-Dec. 2001, doi: 10.1109/54.970422.