150 GHz Differential Amplifiers with Lumped-Elements Matching Networks in 55 nm SiGe BiCMOS

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***Abstract* — This paper presents compact D-band amplifiers in 55 nm SiGe BiCMOS technology. Device models and design tools are first validated with measurements on elementary components above 100 GHz. Then, amplifiers are designed leveraging lumped components in matching networks for minimum area occupation. A differential topology is developed for robustness against parasitic effects of the non-ideal ground, a key issue with lumped components at high frequency. Experimental results are in very good agreement with simulations. The 1-stage amplifier reaches 8 dB gain at 156 GHz and 17.8 GHz bandwidth in 0.026 mm^2 silicon area. The 2-stage amplifier displays 17.4 dB gain at 157 GHz with 42.7 GHz bandwidth in 0.048 mm^2. Compared to previously reported SiGe amplifiers in similar frequency range, more than 2x core area reduction is demonstrated at comparable gain-bandwidth product.**

***Keywords* — D-Band, Amplifier, Millimeter wave integrated circuits, BiCMOS integrated circuits, De-embedding.**

I. Introduction

Advances in silicon technologies enabled integrated circuits operating above 100 GHz. Fundamental building blocks as well as simple transceivers have been demonstrated, particularly in SiGe HBT technologies, and the interest now is rising quickly to exploit the D-band (100-170 GHz) spectrum for practical applications. The ultra-wide usable bandwidth allows wireless communications with a fiber-like transport capacity, key for the infrastructure of future mobile networks [1]. Still, massive use of phased array, i.e. hundreds of active antenna elements, is required to compensate for the high path loss and the limited power delivered from silicon transistors in this frequency range [1]. In such systems, fitting the integrated circuit (IC) size in the area employed by the radiating antenna array is challenging above 100 GHz [2]. In fact, the separation between radiating elements is determined by the wavelength, and the area of the array has to scale down with the square of the wavelength, but the size of the ICs, dominated by front-end amplifiers, is hard to scale proportionally [2].

To achieve enough gain in D-band, where transistors are pushed close to the cut-off frequency, amplifiers require multiple conjugately matched stages. Aside from a few exceptions (e.g. [3]), D-band amplifiers reported so far widely exploit transmission lines (TLINEs) in the matching networks [4]-[8]. TLINEs behaviour is well predictable and less influenced by the surrounding structures, compared to lumped inductors. Moreover, TLINE models are scalable in length and comprise both forward and return current paths, thus making the design robust against the effect of a non-ideal ground plain, crucial at high frequency. Nevertheless, TLINEs occupy a large silicon area, being the wavelength in D-band still relatively high ($\sim$1 mm in silicon), and largely dominate the footprint of amplifiers.

This work presents very compact D-band amplifiers in 55 nm SiGe BiCMOS technology by using lumped components in matching networks. At high-frequency, the effect of current return paths is very critical and difficult to be correctly accounted [11], [12], [13]. To circumvent the issue the amplifiers are designed with a differential topology, with transformers in matching networks, such that no signal current flows through the ground metal plane. The performance predicted by simulations matches very well with experimental results, proving the effectiveness of the preferred strategy. A two-stage amplifier demonstrates gain and bandwidth aligned with state-of-the-art but with at least 2$\times$ area reduction compared to amplifiers leveraging TLINEs in matching networks.

II. Technology

The amplifiers have been designed in STMicroelectronics' 55 nm SiGe BiCMOS technology which offers 8 copper metal layers, 1 aluminum capping layer, metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors. The high speed HBTs feature peak f_t/f_{max} of 320/370 GHz [9]. The technology is well suited for millimeter-wave design, but above 100 GHz the accuracy of the device models as well as the strategies and tools for parasitic estimations are extremely critical. Therefore, elementary components as well as TRL de-embedding structures (thru, reflect, and line) have been designed and fabricated to validate the simulations flow against simple measurements. As an example, Fig. 1 shows the microphotograph of the test structures and the 3D-layout views up to the reference planes for a MOM capacitor and a HBT in common-emitter. Fig. 2 plots the measured results, after de-embedding the access TLINE with the TRL method [10], in comparison with simulations. Only electro-magnetic (EM) simulations are used for the MOM capacitor, while for the HBT the simulations combine the PDK device model, the results of the parasitic extraction tool for the low-level metals, and EM-simulations for the top metals. The plots in Fig. 2(a) show the equivalent capacitance ($C = -\mathrm{Im}[Y_{12}]/\omega$) and the quality factor ($Q = \mathrm{Im}[Y_{12}]/\mathrm{Re}[Y_{12}]$) of MOM capacitor while Fig. 2b reports the Maximum Available Gain (MAG) of the HBT. After fine trimming of the many different simulation tools, the agreement between measurement and simulations is

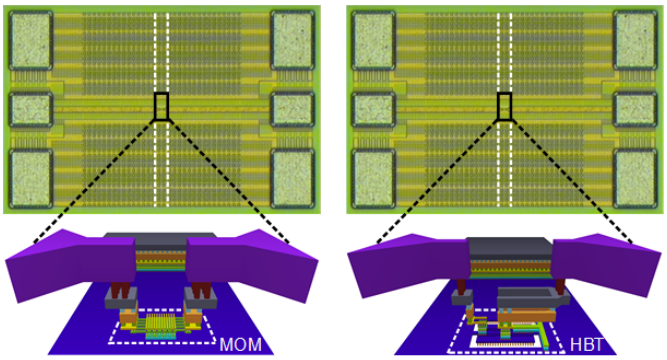

Fig. 1. De-embedding structures for MOM Capacitor and CE HBT.

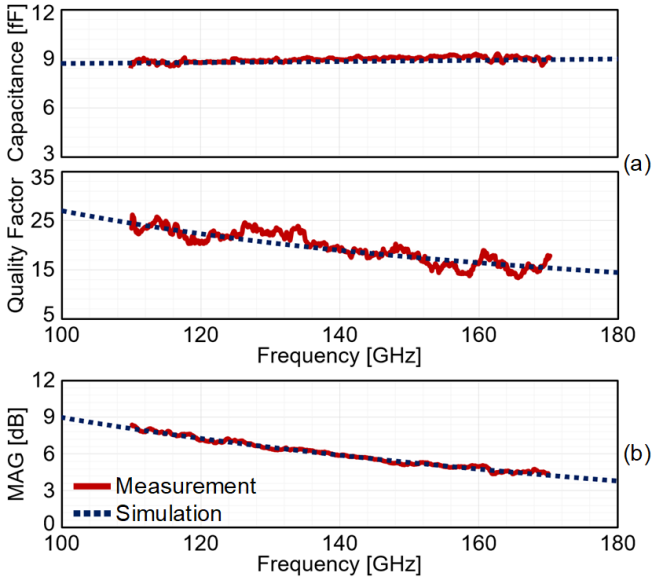

Fig. 2. Comparison of EM simulation and de-embedded measurements: Capacitance of MOM capacitor (top), quality factor of MOM capacitor (center), maximum available gain of transistor in common emitter configuration (bottom).

very good, thus giving high confidence level about reliability of simulations for the design of the amplifiers.

III. Amplifiers Design

The schematics of the D-band amplifiers presented in this paper are shown in Fig. 3. Transistors are employed in CBEBC structure with 0.2 µm × 5.1 µm total emitter area, and the current density is chosen to maximize f_t at 7 mA/µm^2. After optimized layout of metal layers contacting the HBT terminals, the device is unconditionally stable in D-Band, and the f_{max} of the transistor is simulated as 290 GHz. A single transistor in common-emitter configuration exhibits 5.8 dB Maximum Available Gain (MAG) at 150 GHz (consistent with the measurements in Fig. 2) while the stack of two transistors in cascode configuration, with 1.9 V voltage supply, reaches MAG of 13.8 dB. The cascode configuration is therefore selected, allowing more gain than two cascaded common-emitter stages without the necessity of using a bulky inter-stage matching network.

A differential configuration for the amplifiers is selected because, provided symmetry is maintained in layout, a well-

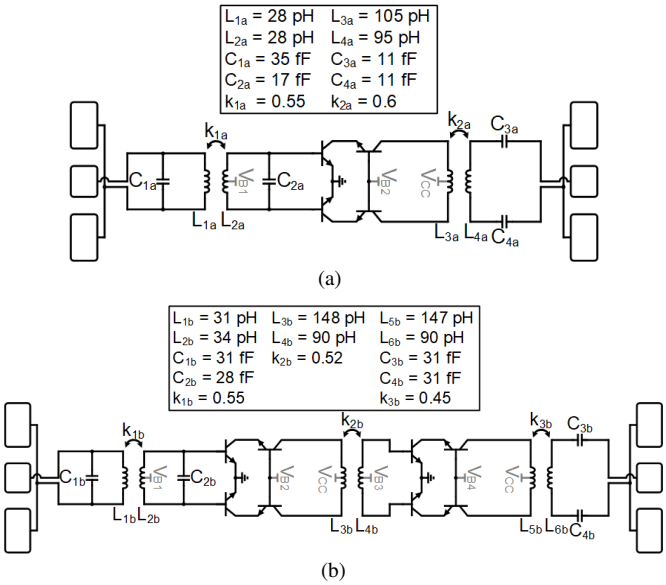

Fig. 3. Schematic of (a) One-stage amplifier, (b) Two-stage amplifiers.

defined virtual ground is established and ideally no signal current flows through the ground plane. This choice avoids the complex and time consuming task of accurate modelling the reactive effects of the ground metal layer in layout [11], [12]. Moreover, in view of active phased arrays with several amplifiers on the same chip, a differential configuration provides common mode noise rejection (e.g. supply and ground noise). Considering the schematic of the 1-stage amplifier in Fig. 3, C_{1a}-C_{2a} with the coupled coils L_{1a}-L_{2a} and C_{3a}-C_{4a} with L_{3a}-L_{4a} form the input and output matching networks respectively, designed to provide conjugate impedance matching to 50 Ω at 150 GHz. The capacitors ($C_{1a\text{-}4a}$), of relatively small value, are implemented with a custom layout as a parallel plate structure with M_3-M_5 metal layers, and precisely sized with electromagnetic (EM) simulations. Being the input and output signals at the GSG pads single-ended, the coupled coils at the input (L_{1a}-L_{2a}) and output (L_{3a}-L_{4a}) perform single-ended to differential conversion and vice versa. The inductors are sized and simulated together with the GSG pad. As an example, Fig. 4 shows the 3D layout of the input transformer (L_{1a}-L_{2a}) connected to the pads. L_{1a} is realized in the two-metal levels below the topmost layer (M_6-M_7) in a stack

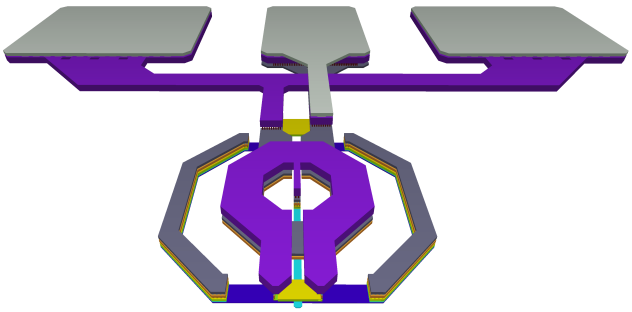

Fig. 4. Layout of the input matching network of one-stage amplifier.

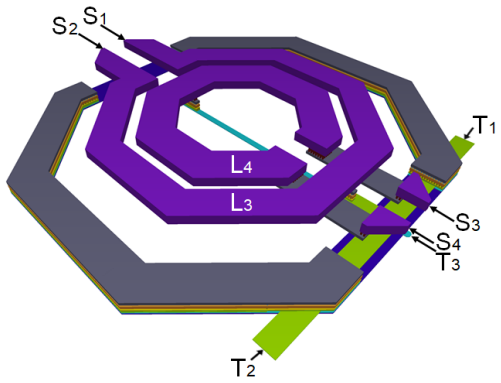

Fig. 5. Layout of the transformer in 2-stage amplifier.

with a diameter of 42 µm and a width of 11 µm. L_{2a} is implemented in the topmost metal layer (M_8) with the same diameter and width of L_{1a}. The center of the L_{2a} is tapped for biasing of input transistors. A side-wall around the coupled inductors, acting as a shield from the surrounding structures in the final amplifier layout, is realized by stacking M_1-M_7 metal layers, and included in the EM simulations. The estimated equivalent inductance (L_{eq}=Im[Z]/ω) of L_{1a} and L_{2a} is 28 pH and the quality factor (Q=Im[Z]/Re[Z]) is 16 and 19 respectively at 150 GHz. The coupling coefficient, defined as $k = \mathrm{Im}[Z_{21}]/\sqrt{\mathrm{Im}[Z_{11}] \cdot \mathrm{Im}[Z_{22}]}$, is 0.55. The layout of the output transformer (L_{3a}-L_{4a}) is similar to L_{1a}-L_{2a} but the spirals are sized such that L_{3a}=105 pH, L_{4a}=95 pH, and k=0.6. The supply voltage for the cascode pair is fed by a center tap on L_{3a}.

In the two-stage amplifier, the input and the output baluns are similar to the single-stage design and an additional transformer is employed as an inter-stage matching network with center taps in primary and secondary coils to provide supply and bias voltage to the first and second stage respectively. The inductors are sized to resonate with the parasitic capacitances of transistors and resonance frequencies are stagger tuned to enlarge the bandwidth. The 3D layout view of the inter-stage transformer is drawn in Fig. 5. Being L_{3b}=148 pH, higher then L_{4b}=90 pH, a planar geometry with both coils in the topmost metal layer is selected giving higher Q ($\sim$20) and self-resonance frequency. A grounded side-wall stacking M_1-M_7 is also included to shield the component.

IV. Experimental Results

The microphotographs of the fabricated amplifiers are shown in the Fig. 6. The core of the one-stage and two-stage amplifier occupies very small area of 116 µm × 220 µm (0.026 mm^2) and 125 µm × 387 µm (0.048 mm^2) respectively.

Small-signal measurement was performed using VDI WR-6.5 D-Band Extenders with Agilent PNA-E8361C vector network analyzer (VNA) and N5260A Millimeter Head Controller. Input and output pads were designed for 75 µm pitch GSG probes. The TRL probe tip calibration has been applied with Cascade standard substrate (138-356).

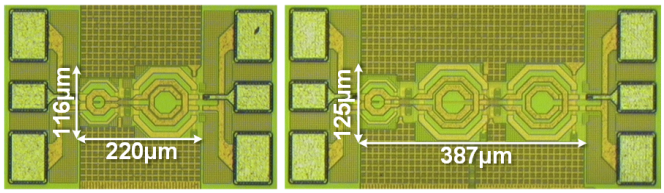

Fig. 6. Chip microphotographs of the one-stage (left) and two-stage (right) amplifiers.

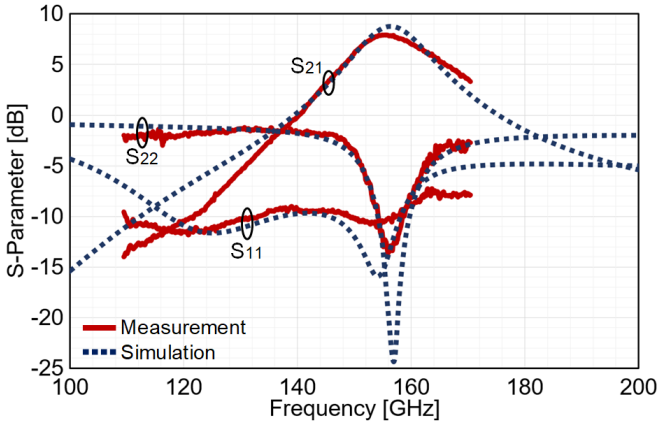

Fig. 7. S-Parameter comparison of measurement and simulation for one-stage amplifier.

Fig. 7 plots the measured S-parameters for the one-stage amplifier (red curves). Drawing 14.2 mA from 1.9 V, the amplifier displays a peak gain of 8 dB at 156 GHz with -3 dB bandwidth of 17.8 GHz. The same plot in Fig. 7 compares measurements against simulations proving an excellent agreement.

S-parameter measurements for the two-stage amplifier are plotted in Fig. 8 (red curves). With 28.4 mA from 1.9 V supply voltage, the amplifier reaches a peak gain of 17.4 dB at 157 GHz with -3 dB bandwidth of 42.7 GHz. Simulations, with dotted lines in the same plots, are still in very good agreement with measurements.

The noise figure (NF) at 150 GHz, derived from simulations, is 11.4 dB and 10.5 dB for the one-stage and two-stage amplifiers, respectively while the output power at 1 dB gain compression is -1.9 dBm and 1.8 dBm.

Finally, Table-I summarizes the measurement results and compares the designed amplifiers against other amplifiers exceeding 100 GHz and designed in SiGe technologies. To the authors' knowledge, [3] was among the first works that demonstrated silicon amplifiers in D-Band and exploited lumped components in matching networks. In comparison with the two-stage amplifier described in this work, the amplifier in [3] features less gain and bandwidth by employing 5 common-emitter stages. [4]–[7] are two-stage amplifiers with cascode HBT configuration and transmission line matching networks. The two-stage amplifier presented in this work has the same HBT configuration and number of stages. Therefore, a direct and fair comparison is possible. The presented two-stage amplifier is highly compact, with 2×

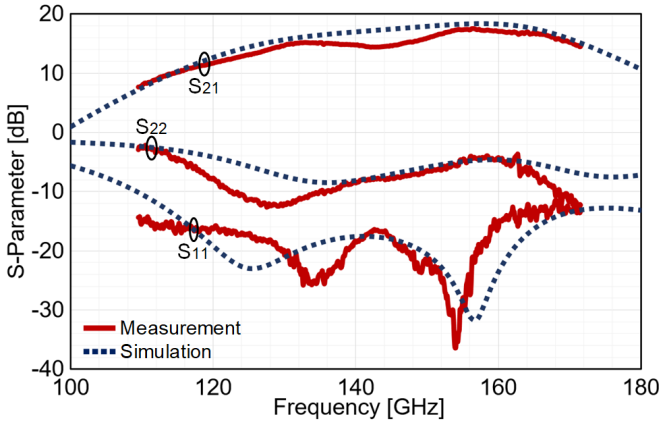

Fig. 8. S-Parameter comparison of measurement and simulation for two-stage amplifier.

Table 1. Comparison with SiGe amplifiers above 100 GHz

	This Work		[3]	[4]	[5]	[6]	[7]
f_t / f_{max} [GHz]	320/370		230/300	250/300	300/500	300/500	300/500
# Stages	1	2	5	2	2	2	2
Gain [dB]	8	17.4	17	25	20.5	27.5	16.1
Center Freq. [GHz]	156	150	140	120	110	125	143
-3dB Bandwidth [GHz]	17.8	42.7	16	20	20	16	11
Gain-Bandwidth Product [GHz]	44.7	316.5	113.3	355.7	211.9	379.4	70.2
P_{DC} [mW]	27	54	112	54	17	12	36.8
Core Area* [mm^2]	0.026	0.048	0.080	0.330	0.220	0.214	0.107

∗Estimated from chip photographs excluding PADs.

or less silicon area occupation. Even though [4] and [6] have slightly higher (1.1× and 1.2×) gain-bandwidth product (GBW), which partially benefit by the lower center frequency, the area occupation is significantly larger (6.9× and 4.5×). Nevertheless, by adding one more stage to the current design the GBW can be significantly increased still maintaining advantage on area occupation.

V. Conclusion

One-stage and two-stage D-Band amplifiers employing lumped-elements matching networks have been designed and fabricated in STMicroelectronics' 55 nm SiGe BiCMOS technology. First, device models and simulation flow are validated with measurements on test structures of elementary components, where the access lines are de-embedded with a TRL calibration kit on silicon. The amplifiers have been designed with differential topology to avoid current return paths through the ground metal layer, challenging to model with sufficient accuracy at high frequency. Measurements on the amplifiers are in excellent agreement with simulations. The two-stage amplifier proved 17.4 dB gain at 157 GHz and 42.7 GHz bandwidth with less than 2× silicon area occupation than previously reported SiGe amplifiers using TLINEs in matching networks. The small amplifier footprint is a key feature in view of dense active phased array transceivers in D-band, where radiating elements are closely spaced.

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