Design of Compact D-band Amplifiers with Accurate Modeling of Inductors and Current Return Paths in 55 nm SiGe BiCMOS

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***Abstract*— This paper presents 1-stage and 2-stage compact D-band amplifiers with lumped-element matching networks implemented in 55 nm SiGe BiCMOS. To correctly account for the effects of a non-ideal ground plane, i.e. reactances in current return paths, and coupling of inductors with nearby layout structures, a shielded 2-port, 4-terminal simulation strategy for inductors is proposed. Validated by measurements, the approach allows very accurate design of compact amplifiers in D-band. The 1-stage design proves 11.8 dB gain at 152 GHz and 17.9 GHz bandwidth in 0.031 mm^2. With the 2-stage amplifier, featuring 20.1 dB gain at 150 GHz with 24.5 GHz bandwidth in 0.058 mm^2, from 2x to 5.7x area reduction is demonstrated against similar SiGe amplifiers in the same frequency band.**

***Keywords*—Amplifier, BiCMOS integrated circuits, Current return path, D-Band, Millimeter wave integrated circuits.**

I. Introduction

Advances in silicon processes enabled ICs operating above 100 GHz. Fundamental building blocks as well as complete transceivers have been demonstrated, particularly in SiGe HBT technologies, and the interest is now growing fast to exploit the D-band (110-170 GHz) spectrum for practical applications, where the ultra-wide available bandwidth enables wireless communications with a fiber-like transport capacity. A massive use of phased array, i.e. hundreds of radiating elements, each one driven by a dedicated front-end, is foreseen to compensate the high path loss and the limited available power from a single element [1]. To this purpose, a key challenge beyond 100 GHz is to fit the ICs in the area occupied by the antenna array [2]. In fact, the separation between radiating elements is set by the wavelength, but while the area of the antenna array shrinks with the square of the wavelength, the size of the ICs, dominated by the many required amplifiers, is hard to scale proportionally [2] motivating investigations to shrink the size.

In D-band, amplifiers need multiple stages, conjugately matched to maximize gain. Apart few exceptions (e.g. [3]) amplifiers reported so far leverage transmission lines (Tlines) in matching networks [4]-[8]. The good confinement of the electromagnetic field in Tlines limits coupling and cross-talk issues with nearby components, while the structured Tline models, accounting both forward and return current paths, make the design robust against the effects of a non-ideal ground plane, a critical issue at high frequency. However, despite the short wavelength in D-band, Tlines occupy large area and represent the primary limit to scale the size of active circuits.

The amplifiers footprint can be drastically reduced with compact inductors in matching networks, as commonly used in the lower portion of the millimetre-wave band [9]. However, inductors are influenced from coupling with nearby structures in layout. Moreover, the effects of current return paths [10],[11], must be carefully accounted in D-band to avoid unpredicted networks mistuning, responsible of frequency shift or loss of gain.

This work investigates the issue and proposes an accurate, yet simple, strategy for design and modelling of inductors at very high frequency without the need of performing complex electromagnetic (EM) simulations on large portions of the layout. Inductors are surrounded and co-simulated with a metal shield which ensures the component is unaffected by couplings with nearby structures. Moreover, inductors are considered as 2-port, 4-terminal devices, similar to Tlines, such that both the forward and return current paths can be accurately accounted. The approach is exploited and validated by designing 1-stage and 2-stage compact D-band amplifiers in a SiGe BiCMOS 55 nm technology. Provided inductors are correctly simulated, the predicted amplifiers performance matches very well with measurements, proving the validity of the proposed strategy. Moreover, the 2-stage amplifier demonstrates from 2x to 5.7x silicon area reduction compared to Tline-based amplifiers giving comparable gain-bandwidth product in the same frequency range.

II. D-band Amplifiers Description

The schematics of the D-band amplifiers are drawn in Fig.1. The circuits are designed and realized in STMicroelectronics 55 nm SiGe BiCMOS technology, featuring 8 copper metal layers, 1 aluminum capping layer, metal-insulator-metal (MIM), metal-oxide-metal (MOM) capacitors and high speed HBTs with peak f_t/f_{max} of 320/370 GHz. The chip photographs of the realized amplifiers are shown in Fig. 2. The amplifiers are very compact with core area (excluding pads) of 138 µm x 228 µm (0.031 mm^2) and 256 µm x 228 µm (0.058 mm^2) respectively.

The two amplifiers use the same HBT of 5.1 µm x 0.2 µm total emitter area. After careful layout, and biased with 7.1 mA collector current, the simulated f_{max} of the HBT is 290 GHz. A single HBT in common-emitter (CE) with V_{CE}=1V displays Maximum Available Gain (MAG) of 5.8 dB at 150 GHz while the cascode configuration, supplied at 1.9 V, reaches 13.8 dB MAG. Considering the target of minimizing the amplifiers footprint, the cascode structure is finally selected, enabling more gain than two cascaded CE stages without the need for a bulky interstage matching network.

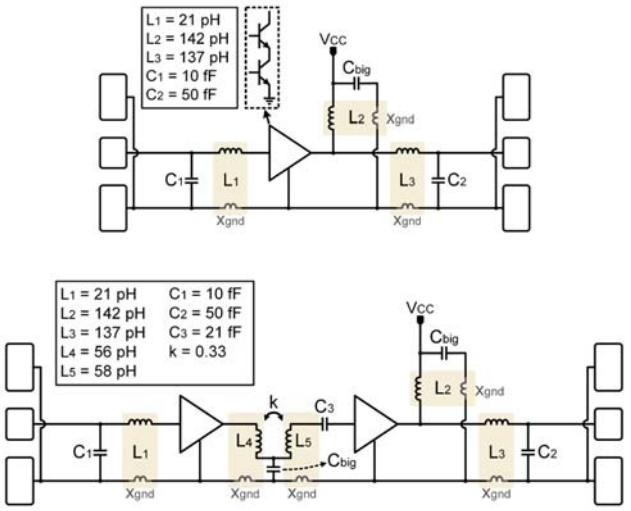


Fig.1. 1-stage (top) and 2-stage (bottom) amplifiers schematic. x_{gnd}, coupled with nearby inductors, represents current return paths.

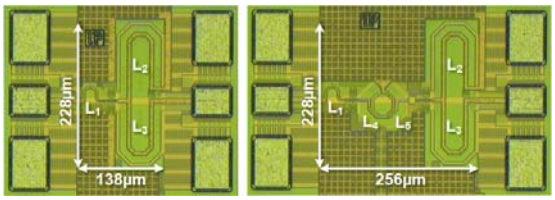
Looking at the amplifiers schematics in Fig. 1. C_1-L_1 and C_2-L_2-L_3 form input and output matching networks respectively, identical in the one- and two-stage amplifiers. The networks are designed to provide conjugate impedance matching to 50 Ω at ~150 GHz. C_1 and C_2, of relatively small value, are realized with M_3-M_5 metal layers as parallel plate capacitors and accurately sized with EM simulations.

Inductors L_1, L_2, L_3 are realized in the topmost metal layer and laid out with U shape, as visible in the chip photographs in Fig. 2. For the largest inductors (L_2, L_3) the U shape yields ~30% higher quality factor and ~10% higher self-resonance frequency compared to a multi-turn layout. Because of the small footprint, metal density rules are satisfied without adding tiles in close proximity with the inductors. No substrate shield is used, having negligible effect in this frequency range.

In the two-stage amplifier (bottom schematic of Fig.1), C_3 and the magnetically coupled inductors L_4-L_5 implement the inter-stage matching network, stagger tuned to flatten the amplifier frequency response. L_4-L_5 are wounded and form a coplanar transformer with k=0.33.

The reactances x_{gnd} in the schematics of Fig.1 represent non-ideal current return paths and are enclosed in a shadowed area to highlight coupling with the corresponding inductors. The approach followed for modelling inductors and x_{gnd} is deeply discussed in the next section.

Finally, capacitors for supply decoupling (C_{big} in Fig. 1) also deserve attention. C_{big} must provide low impedance (ideally a short circuit) to the grounding point in the layout at the amplifier center frequency. But being of large value the self-resonance frequency has to be considered carefully. C_{big} are realized by stacking MIM and MOM capacitors for maximum density, i.e. maximum capacitance with minimum parasitic access inductance. The stack is sized to have the self-resonance frequency near the amplifiers center frequency. From EM simulations, C_{big} presents an impedance below 1 Ω from 114 to 168 GHz with minimum value of 0.3 Ω at 140 GHz.



(a) (b)

Fig. 2. Chip photograph of the (a) 1-stage and (b) 2-stage amplifiers.

III. Inductors and Currents Return Path

The key issues of managing inductors in D-band is taking into account the effects of the surrounding layout (i.e. other components, metals and ground plane) and currents return path. At lower frequency, where the above effects have a minor impact, coupling with nearby layout structures is typically neglected and a common ideal and shared reference (ground) is assumed in the model of the inductors [9].

The limitations of this approach in D-band are quantitatively analyzed in this section and a robust implementation and modeling strategy is finally proposed. We keep as an example inductor L_3, used in the output matching network. Fig. 3 shows the layout and the current distribution at 150 GHz, derived from EM simulations, in different cases. Fig. 4 presents the corresponding lumped-element models (loss resistors are included in series to each component but not shown for better readability) while Fig. 5 plots the simulated and modelled equivalent inductance over frequency.

In Fig. 3a the inductor L_3 (realized in the top Cu metal, M8) is simulated as a 3-terminal device: S_1, S_2 are EM-ports at the inductor ending points while G is a port on a substrate tap to account for coupling toward the substrate. This approach is accurate if no other structures or metals are close to the inductor and assumes ideal current return paths (i.e. a shared ground node). The inductor behavior is reproduced by the simple equivalent circuit in Fig. 4a, where the two capacitors C_1 account for substrate coupling. The equivalent inductance, L_{eq}=Im[Z]/ω (with Z the impedance between terminal S_1 and terminal S_2 shorted to G) is plotted in Fig. 5 and shows a self-resonance frequency above 240 GHz. The simulated quality factor at 150 GHz (not shown) is Q=28.

Fig. 3b shows a more realistic situation where a uniform metal is included around the inductor to mimic the effect of the ground distribution plane in final layout. The distance to the edge of the inductor is set to 3 times the width of the M8 trace and the inductor is still considered as a 3 terminal device. As evident from the colors of the current density plot, an intense current is induced by the top M8 trace on the edge of the surrounding metal, suggesting that coupling between the inductor and nearby structures cannot be neglected at all. On the other hand, the same plot reveals that the induced current drops very quickly moving away from the edge of the surrounding metal, suggesting the latter can be exploited to shield very well the inductor from the rest of the layout. The inductor behavior is then robust against ground plane

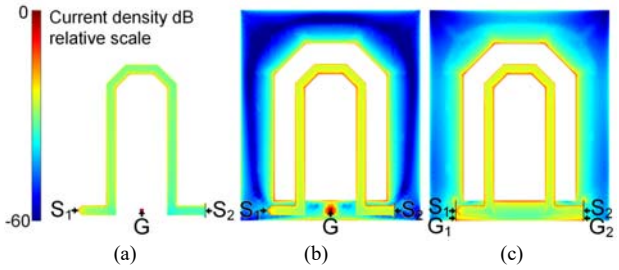


Fig. 3. Inductor layout with current density from EM simulations. (a) 3-terminal without shielding, (b) 3-terminal with a surrounding metal layer, (c) 4-termianl to include current return path.

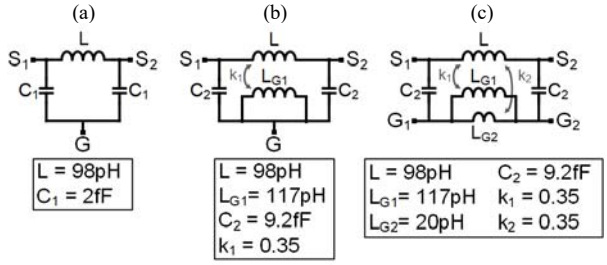


Fig. 4. Equivalent circuit models reproducing EM simulations for the three situations in Fig. 3.

discontinuities slightly away from the edge such as metal slots for density rules or wires for biasing and controls. In the equivalent circuit model, Fig.4b, the effect of the surrounding metal layer is captured by an additional inductor (L_{G1}) coupled to the main inductor (L) and larger capacitances to the G node (C_2). Compared to the previous case (Fig.3a and Fig.4a), the self-resonance frequency of the equivalent inductance, plotted in Fig.5, is now reduced to around 178 GHz. The simulated quality factor at 150 GHz is 17.

By designing and simulating the inductor as in Fig.3b, the quality factor is penalized, but the component behavior will not be affected by other layout structures that may be in close proximity. However, with a single lumped reference port (G), the parasitic reactance of the current return path (x_{gnd} in the schematics of Fig.1) is not yet considered. In D-band, grounding taps located on different places in the layout cannot be assumed as perfectly short-circuited. Therefore, inductors are considered 4-terminal devices and simulated as shown in Fig. 4c. S_1, S_2 and G_1, G_2 (ports in EM simulations) are placed respectively on the inductor ending points and on the ground metal layer just below S_1, S_2. By looking at the current density in Fig.3c, a significant current flows straight in the return path, from G_2 to G_1. The 4-terminal inductor equivalent circuit is represented in Fig. 4c where, in comparison with Fig.4b an additional coupled inductor, L_{G2}, is included to model the return path from G_2 to G_1. Curve (c) in Fig.5 plots the equivalent inductance, derived from the impedance between S_1 and G_1 terminals with S_2 shorted to G_2. The self-resonance frequency is around 192 GHz and in the 140-160 GHz (the target bandwidth of the amplifiers) the equivalent inductance falls in the middle between the values predicted by the simplified simulation approaches in Fig.3a and 3b. The estimated quality factor is roughly the same as for the case in Fig. 3b. The importance of careful inductors modeling and the accuracy of

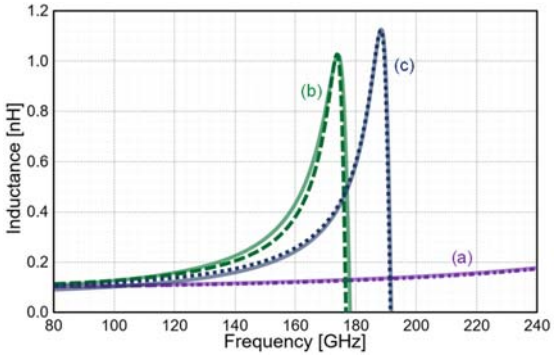


Fig. 5. Equivalent inductance from EM-simulations and lumped circuit models for the three situations in Fig. 3.

the 4-terminal approach is confirmed by comparing measurements of the amplifiers against circuit simulations, performed by modeling the inductors with the 3 approaches of Fig.3, in the following section.

IV. Experimental Results

Small-signal measurement was performed using VDI WR-6.5 D-Band Extenders with Agilent PNA-E8361C vector network analyzer (VNA) after thru-reflect-line (TRL) probe tip calibration. Fig. 6 plots the measured S-parameters for the one-stage amplifier (red curves). Drawing 7.1 mA from 1.9 V, the amplifier displays a peak gain of 11.8 dB at 152 GHz with -3dB bandwidth of 11.8 GHz. The same plot compares measurements against simulations, performed by modelling the inductors as discussed in the previous section. *sim.(a)* neglects coupling of inductors with nearby metals and currents return path. *sim.(b)* considers a metal loop around inductors but still neglects currents return path while *sim.(c)* considers both effects. The remarkable discrepancy between measurements and *sim.(a)*, *sim.(b)* and the very good agreement with *sim.(c)* confirms the importance of careful inductors modelling and validate the proposed approach. EM simulations for the full layout (excluding HBTs) were also performed and results are in agreement with the much faster *sim.(c)* approach.

S-parameter measurements for the 2-stage amplifier are plotted in Fig. 7 (red curves). With 14.2 mA from 1.9 V supply voltage, the amplifier reaches a peak gain of 20.1 dB at 150 GHz with -3 dB bandwidth of 24.5 GHz. Also in this case measurements are in good agreement with *sim.(c)* while a remarkable discrepancy is evident with *sim.(a)* and *sim.(b)*.

Finally, measurement results are summarized in Table-I and compared against other SiGe HBT amplifiers above 100 GHz. [3] was among the first works demonstrating silicon amplifiers in D-band (to Authors knowledge). The amplifier, with 5 CE stages and based on lumped-component matching networks, features lower gain with less bandwidth and larger area occupation than the 2-stage amplifier presented in this work. [4-7] are two-stage cascode amplifiers with Tlines matching networks. Having the same number of stages and the same transistors configuration of the presented 2-stage amplifier, a fair performance comparison is possible. The presented amplifier is extremely compact, with 2x to 5.7x area

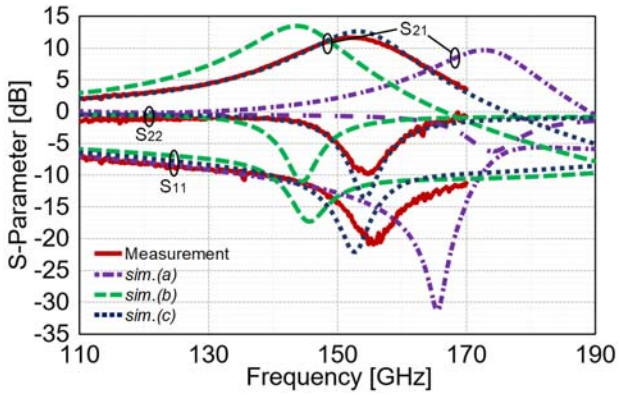


Fig. 6. 1-stage amplifier measurement and comparison with simulations. (*sim.(a)*: unshielded inductors and lumped ground, *sim.(b)* shielded inductors and lumped ground, *sim.(c)* shielded inductors and current return paths included).

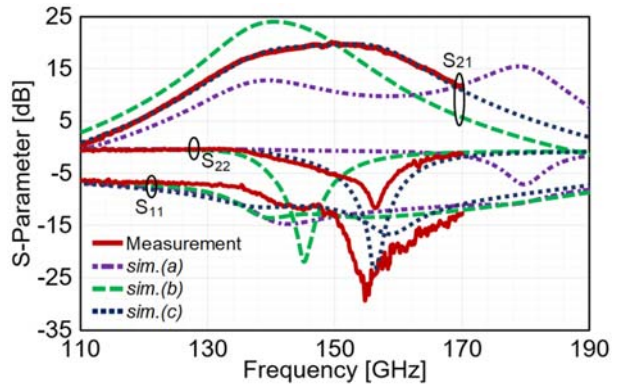


Fig.7. 2-stage amplifier measurement and comparison with simulations. (*sim.(a)*: unshielded inductors and lumped ground, *sim.(b)* shielded inductors and lumped ground, *sim.(c)* shielded inductors and current return paths included).

reduction in comparison with [4-7]. The slightly higher gain-bandwidth product (GBW) of [4],[6] (1.4x -1.5x) is at the cost of a remarkably larger area occupation (3.7x - 5.7x) and can be reached by adding one stage to the proposed design, still maintaining substantial advantage in area occupation.

V. Conclusion

D-band amplifiers in SiGe BiCMOS technology with lumped components in matching networks have been presented. To account for the effects of a non-ideal ground, i.e. reactance of current return paths and couplings with nearby metal layers in layout, inductors are shielded and modelled as 4-terminal devices. The approach, validated by the good agreement between measurements and simulations, enables a robust and reliable design of compact amplifiers, key for future development of dense phased-array systems in D-band. The presented 2-stage amplifier reaches 20.1 dB gain at 150 GHz and 24.5 GHz bandwidth with 2x or more silicon area saving compared to SiGe HBT amplifiers using transmission lines for matching networks.

TABLE-I: Comparison with SiGe amplifiers above 100GHz

	This Work		[3]	[4]	[5]	[6]	[7]
f_t / f_{max} [GHz]	320/370		230/300	250/300	300/500	300/500	300/500
# Stages	1	2	5	2	2	2	2
Gain [dB]	11.8	20.1	17	25	20.5	27.5	16.1
Center Freq. [GHz]	152	150	140	120	110	125	143
-3dB Bandwidth [GHz]	17.9	24.5	16	20	20	16	11
Gain-Bandwidth Product [GHz]	69.6	247.8	113.3	355.7	211.9	379.4	70.2
P_{DC} [mW]	13.5	27	112	54	17	12	36.8
Core Area* [mm^2]	0.031	0.058	0.080	0.330	0.220	0.214	0.107

* Estimated from chip photographs excluding PADs

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References

[1] M. G. L. Frecassetti, A. Mazzanti, J. F. Sevillano, D. del Río and V. Ermolov, "D-Band Transport Solution to 5G and Beyond 5G Cellular Networks," 2019 European Conference on Networks and Communications (EuCNC), Valencia, Spain, 2019, pp. 214-218.

[2] B. Sadhu, X. Gu and A. Valdes-Garcia, "The More (Antennas), the Merrier: A Survey of Silicon-Based mm-Wave Phased Arrays Using Multi-IC Scaling," in IEEE Microwave Magazine, vol. 20, no. 12, pp. 32-50, Dec. 2019.

[3] E. Laskin, P. Chevalier, A. Chantre, B. Sautreuil and S. P. Voinigescu, "80/160-GHz Transceiver and 140-GHz Amplifier in SiGe Technology," 2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Honolulu, HI, 2007, pp. 153-156.

[4] G. Liu and H. Schumacher, "47–77 GHz and 70–155 GHz LNAs in SiGe BiCMOS technologies," 2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Portland, OR, 2012, pp. 1-4.

[5] A. Ç. Ulusoy, M. Kaynak, V. Valenta, B. Tillack and H. Schumacher, "A 110 GHz LNA with 20dB gain and 4dB noise figure in an 0.13µm SiGe BiCMOS technology," 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), Seattle, WA, 2013, pp. 1-3.

[6] A. Ç. Ulusoy et al., "A SiGe D-Band Low-Noise Amplifier Utilizing Gain-Boosting Technique," in IEEE Microwave and Wireless Components Letters, vol. 25, no. 1, pp. 61-63, Jan. 2015.

[7] J. Heredia et al., "A 125–143-GHz Frequency-Reconfigurable BiCMOS Compact LNA Using a Single RF-MEMS Switch," in IEEE Microwave and Wireless Components Letters, vol. 29, no. 5, pp. 339-341, May 2019.

[8] E. Turkmen, A. Burak, A. Guner, I. Kalyoncu, M. Kaynak and Y. Gurbuz, "A SiGe HBT D-Band LNA With Butterworth Response and Noise Reduction Technique," in IEEE Microwave and Wireless Components Letters, vol. 28, no. 6, pp. 524-526, June 2018.

[9] T. O. Dickson et al.:, "30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," in IEEE Trans. on Microwave Theory and Techniques, vol. 53, no. 1, pp. 123-133, Jan. 2005.

[10] H. Wang, L. Zhang, D. Yang, D. Zeng, Y. Wang and Z. Yu, "Modeling of Current-Return-Path Effect on Single-Ended Inductor in Millimeter-Wave Regime," in IEEE Electron Device Letters, vol. 32, no. 6, pp. 737-739, June 2011.

[11] Y. Zhu et al., "An Equivalent Circuit Model With Current Return Path Effects for ON-Chip Interconnect up to 80 GHz," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 5, no. 9, pp. 1320-1330, Sept. 2015.