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Summary

This report presents the design and characterization results of the I/Q modulator and SPI interface of the D-band radio transceiver. The I/Q modulator is a key block for our system especially because we want to achieve the highest level of modulation. For this purpose, an I/Q modulator has been developed to convert the baseband signal to D-band while maintaining the best signal quality by getting the best compromise between linearity, LO rejection and image rejection. The SPI interface is used to control the circuits from the outside, in order to easily adjust the bias currents, phase shifts, operation frequency and so on.

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Contents

List of Acronyms and Abbreviations

DAC	Digital to Analog Converter
DC	Direct Current
DDAT	Double Distributed Active Transformer
EC	European Commission
fFDD	flexible Frequency Division Duplex
FDD	Frequency Division Duplex
FP7	Seventh Framework Program
ICT	Information and Communication Technologies
IF	Intermediate Frequency
IIP3	Third order intercept point –input referred
IIP5	Fifth order intercept point – input referred
IM3	Third order intermodulation
IP1dB	1-dB compression point – input referred
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MIM	Metal-Insulator-Metal
MISO	Master input, slave output
MMIC	Monolithic Microwave Integrated Circuit
mmW	Millimeter Wave
MOSI	Master output, slave input
MSB	Most Significant Bit
NF	Noise Figure
OIP3	Third order intercept point – output referred
OIP5	Fifth order intercept point – output referred
OP1dB	1-dB compression point – output referred
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PC	Personal Computer
PLL	Phase Locked Loop
RF	Radio Frequency
RSTN	Active low reset
RX	Receiver
SBC	Single Board Computer
SCK	Serial Clock
SMD	Surface Mounted Device
SPI	Serial Peripheral Interface
SS	Slave Select
TDD	Time Division Duplex
TX	Transmitter
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio

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1. Introduction

Tasks 2.1 and 2.2, defined in the project proposal, related to the D-band analog transceiver functional block design, frequency synthesizer included, have a central role within the WP2 for the development of the D-band backhaul transceiver in the DREAM project. D2.1 and D2.2 deliverables are the first report of WP2, being focused to the functional block feasibility studies and to the design approach activities of task 2.1 and 2.2. D2.3 deliverable present the design and the characterization of the I/Q converter and the SPI interface for control and monitoring, which are the last blocks (frequency synthesizer excluded) that are not covered by D2.1 and D2.2.

The tasks 2.1 and 2.2 provide the D-band transceiver front-end building blocks, implemented in ST's advanced BiCMOS process, to the task 2.3, where all of these IPs are properly interfaced and integrated to build up the complete D-band backhaul radio transceiver front end chip set for antenna array beam forming. For such an application, it is worthwhile to remind three performance figures of utmost importance:

1. the transmitter, including the antenna array directivity, must provide a relatively high output power, to cover distances up to 300 meters;
2. the receiver, including the antenna array directivity, must provide a relatively high sensitivity, to cover distances up to 300 meters;
3. the phase shifter to properly vary the phase of the incoming carrier frequency and then steer the antenna beam;
4. the LO synthesizer phase noise, enabling high spectral efficiency modulation schemes. The characterization of the frequency synthesizer multiplier, designed by UniPV, are described in the D2.5 deliverable document

The IQ modulator launched for fabrication in the second tape-out has been extensively characterized and the performances have been compared together with the final requirements in the deliverable D1.5. The SPI interface for control and monitoring has been completely tested and verified, validating its suitability for the final demonstrator.

2. I/Q upconverter

2.1 Introduction

The Figure 1 shows the D-band direct conversion transmitter functional diagram, where the TX functional description starts from the left blocks to the right ones. The digital bit stream outputted from the Modem, which implements the proper modulation order function is converted by the two DAC in the in-phase (I) and the quadrature-phase (Q) components of the message analog modulating signal. The baseband signal is directly mixed with the local oscillator carrier frequency (VCO) by the two quadrature mixers to get the up-conversion to the modulated carrier in the D-band frequency range around 150GHz. The up-converted RF signal is then amplified and distributed by N-way power splitter to the active antenna array system. The satellite IC drives 4 antenna array elements each by phase shifting and power amplifying the modulated carrier frequency in D-band.

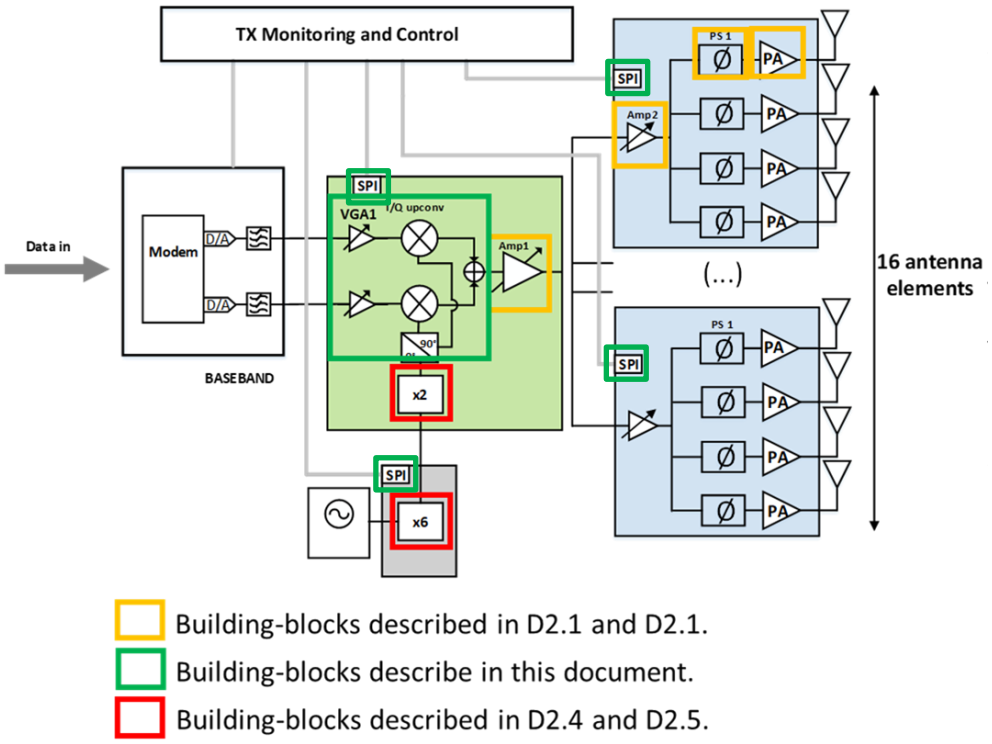

Figure 1: D-band transmitter analog front-end block diagram

As shown in Figure 1, the I/Q modulator in green rectangle is the last RF building block not yet described in earlier reports. It is a key block that up-convert the wideband I/Q signals to D-band while maintaining the quality of the signal.

The results of all other RF blocks, including the power amplifier (PA), low-noise amplifier (LNA), variable amplifier, phase shifter, D-band doubler and the multiplier by 6 have already been presented in documents D2.1, D2.2, D2.4 and D2.5.

2.2 General description

This chip is fed by the baseband I/Q signals from the modem and the single-ended LO in D-band and produces at its output the D-band signal to be transmitted. For this chip, there is no size constraint.

As described in Figure 2, it consists of two double balanced-mixer, a quasi-differential LO-driver and a RF buffer to achieve the targeted conversion gain. The differential I/Q buffers have been implemented to interface the output signals from the modem to the up-converter. As all circuits are differential or quasi-differential, two Marchand baluns have been designed and implemented in addition (named S2D in the block diagram). The output matching circuit ensures a good power transfer between the mixer and the RF amplifier to get wideband performances.

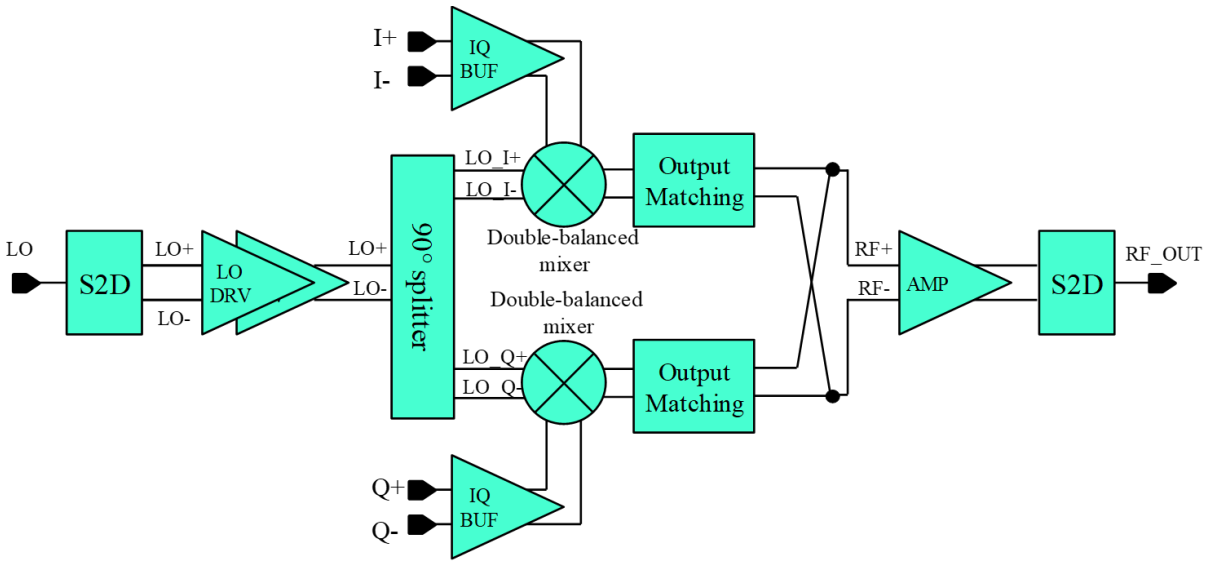

Figure 2: Block diagram of the up-converter.

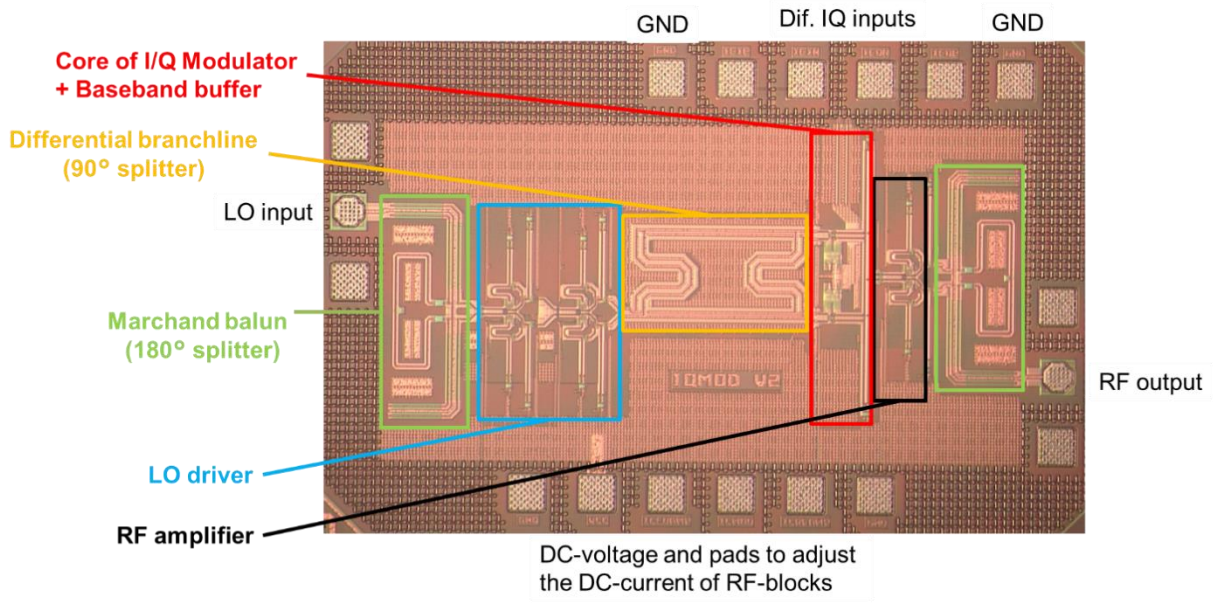

Figure 3: Microphotograph of upconverter.

A chip microphotograph of our upconverter is shown in Figure 3. Even if there is no size constraint, the chip size including the pads and the seal ring is only 1.28 x 0.84 mm².

To maintain the performances of the upconverter, the layout has been carefully done to maintain the symmetry and the phase difference between quadrature and differential signals. The microstrip transmission lines are composed of a thick top layer as a signal conductor, and a ground conductor that can be one or several interconnect layers.

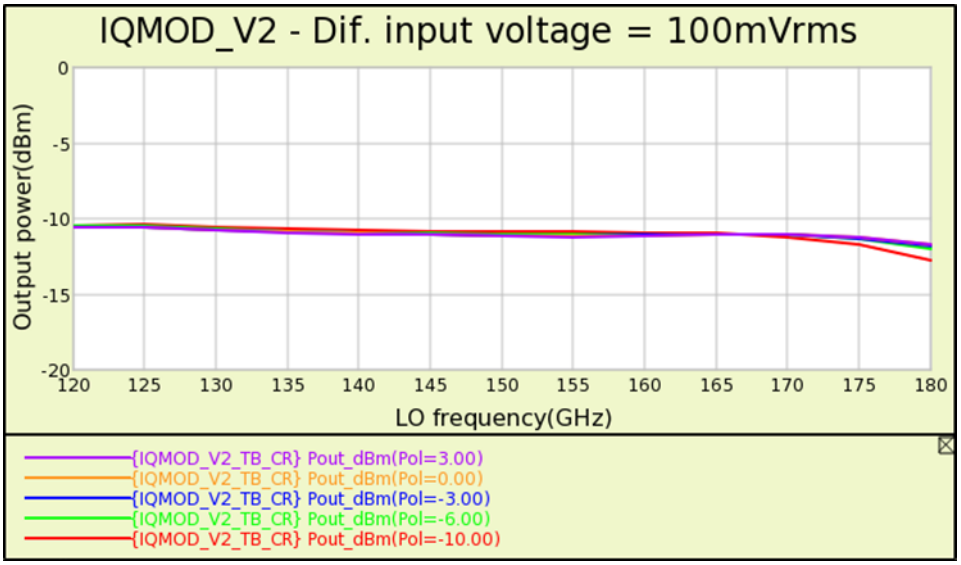

Figure 4: Output power vs LO frequency and LO level.

As we are working in D-band, all passive parts who play a role in D-band have been simulated with the EM simulator and added in the schematic to obtain the simulation results of the output power shows in Figure 4. As targeted for this functional block, the output power is around -12dBm from 120GHz to 170 GHz for a large range of LO level (from -10 dBm to 3 dBm).

2.3 D-band scalar test bench to characterize the up-converter

In order to be able to characterize the I/Q up-converter, a new test bench has been setup using Anritsu's new spectrum analyzer (MS2760A) which allows a complete broadband coverage from 9 kHz to 170 GHz without the need of an external mixer.

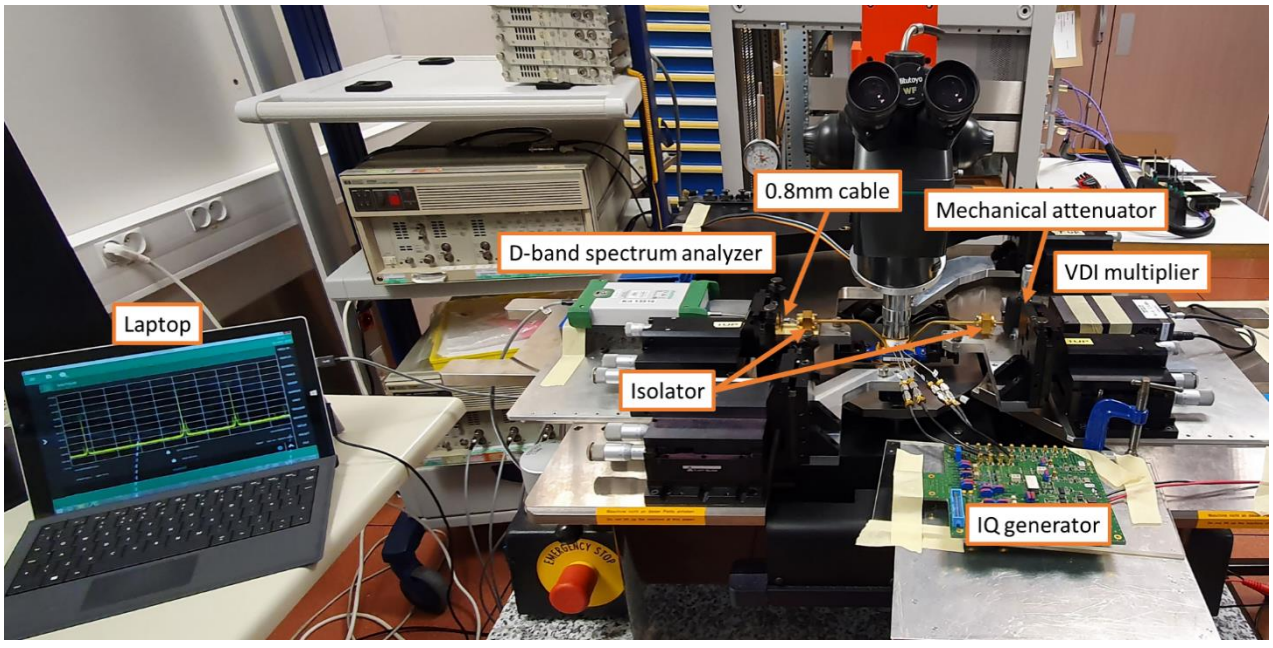

Figure 5: Photography of the test bench

As shown in Figure 3, the LO signal in D-band is generated from a signal synthesizer followed by a VDI multiplier by 6 and a mechanical attenuator to adjust the LO level from -20 to 5 dBm.

The spectrum and output power are directly measured with the spectrum analyzer. All insertion losses of the measurement setup are calibrated out, but not the mismatch losses. The current configuration allows to characterize the circuit for a LO frequency between 120 GHz and 168 GHz.

Depending on the tests to be carried out, several solutions are used to generate the I and Q signals at the input of the modulator. On the picture of the test bench, it is a board developed by NOKIA which allows to generate the I and Q signals with an amplitude of 50mVrms (100mVrms differential) at 20 MHz and a common mode voltage around 2.4 Volt. The DC offsets on the I and Q signals can be tuned to reduce the OL leakage on the RF port.

For instance, the LO input and RF output losses are 3.5 dB and 6.5 dB respectively at 150 GHz. The poor return loss of the spectrum analyzer in D-band generate mismatching that is not taken account.

During the tests, the chips were glued on a base to remove uncertainty about the quality of RF probe contact on sawed chips and improve repeatability of the measurements.

2.4 Measurement results

Below is a measured D-band output spectrum based on the test bench described in section 92.3. In this configuration, the upper sideband has been selected. The total power of the I and Q signals at 20 MHz is -7.5 dBm and the common mode voltage is 2.4 Volt. The spectrum is clean and the uncalibrated LSB, LO and USB output powers are -65 dBm, -39 dBm and -27.5 dBm respectively, giving a LO rejection at RF-port of 10 dBc and an image rejection of 25 dBc.

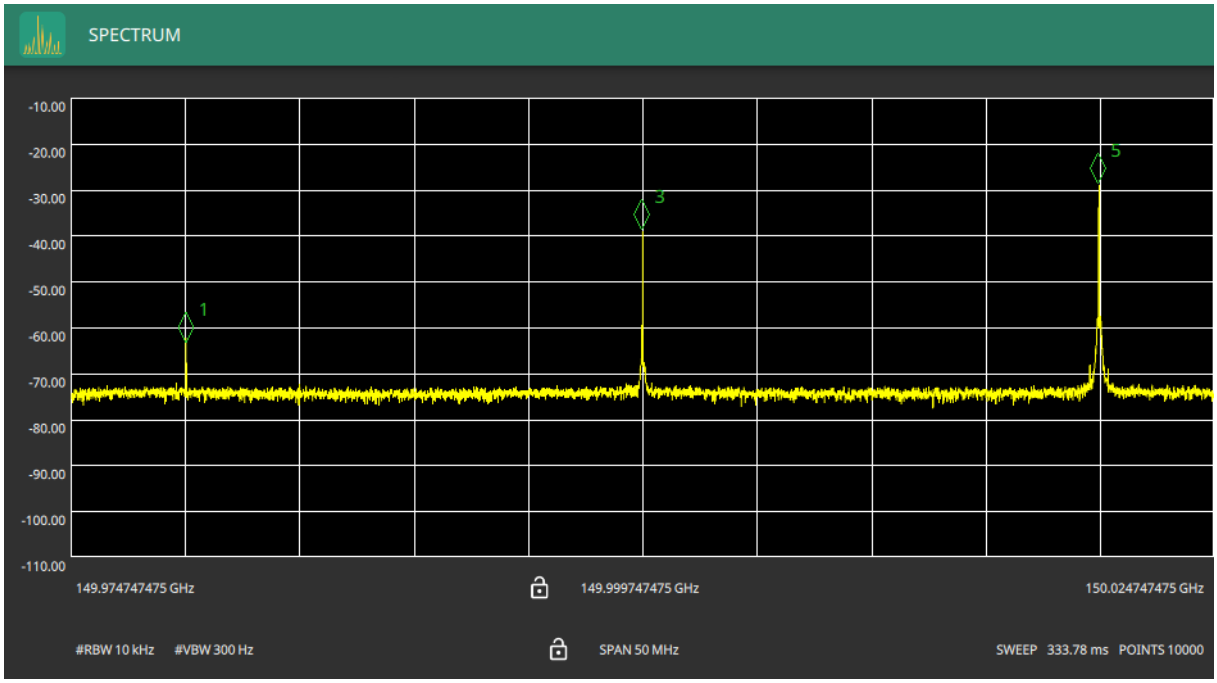

Figure 6 : Typical output spectrum at LO freq. = 150 GHz and LO level = 0 dBm.

By tuning the DC offset of the I and Q signals, it is easy to improve the LO rejection without modifying the LSB and USB signals as shown on Figure 7. A DC offsets of 36 mV on channels I and Q is enough to improve the LO rejection by more than 30 dB.

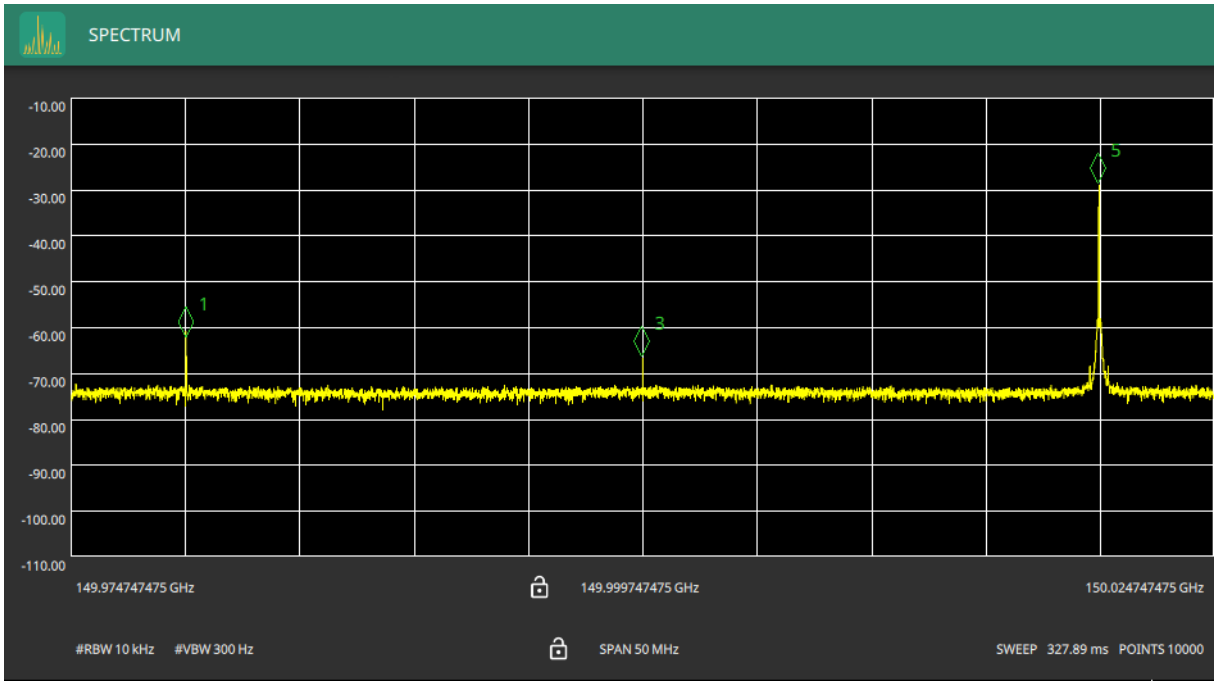

Figure 7 : Typical output spectrum at LO freq. = 150 GHz, LO level = 0 dBm and DC offset to cancel the LO.

In order to be able to make measurements as a function of the frequency and power of the I and Q signals, the board to generate the I/Q signals is replaced by an RF generator followed by an external 90° hybrid coupler and two external 180° hybrid couplers. The output spectrum of the Figure 8 shows that in this new configuration, the lower sideband is selected.

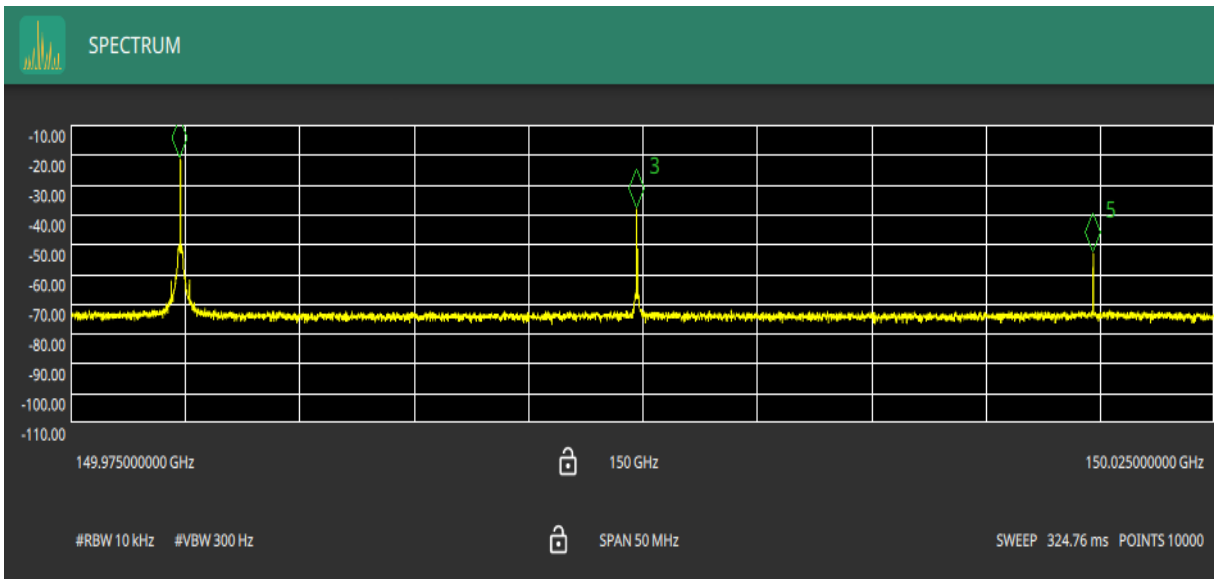

Figure 8 : Typical output spectrum at LO freq. = 150 GHz, LO level = -5 dBm and a total power of 20 MHz I/Q signal = -1.5 dBm.

As the input signal was increased by 6 dB, the LO rejection and image rejection are 6 dB better i.e. 16 dBc and 31 dB for LO and image rejection. Taking into account the output insertion loss of 6.5 dB, the output power of the main tone is -20 dBm + 6.5 dB = -13.5 dBm and then the conversion gain is equal to -12 dB.

The next measurement was performed to evaluate the sensitivity at the LO input level (see Figure 9). Performance is relatively stable if the LO level is above -10 dBm, which gives us the minimum level that the D-band doubler should provide to the I/Q modulator.

Figure 9 : Measurement results versus LO power.

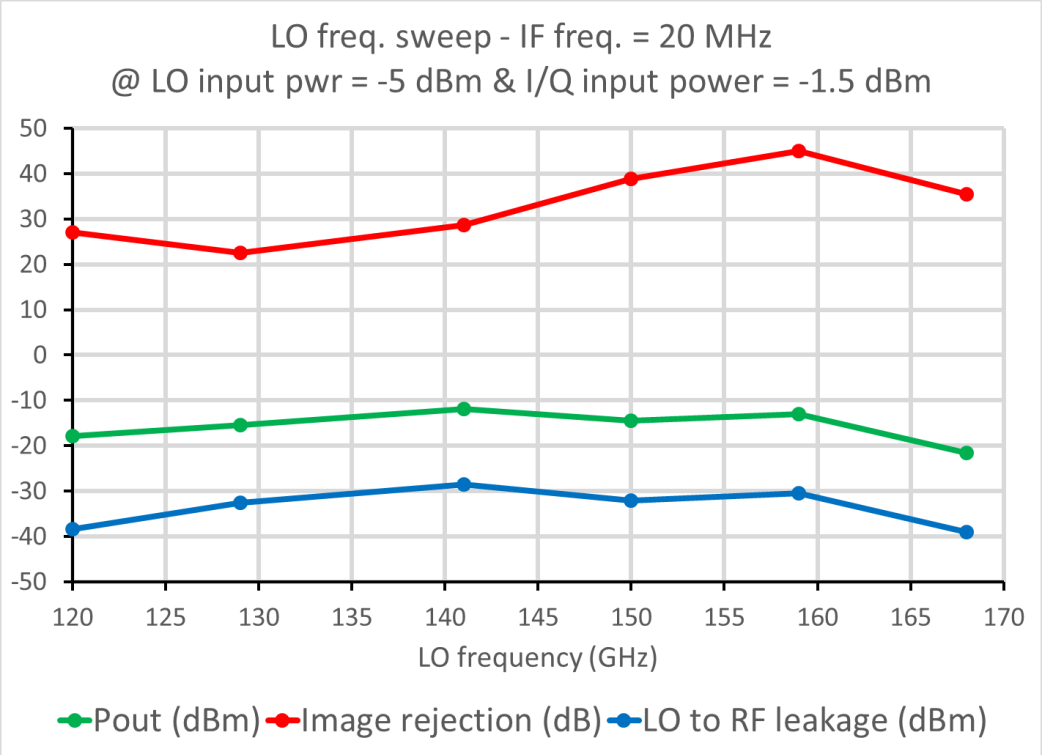

Figure 10 : Measurement results versus LO frequency (uncalibrated).

The performance of the modulator is broadband and covers at least the range 130Ghz-160 GHz, i.e. more than 20% (see Figure 10) even if the best performance is obtained in the DREAM band (140 GHz to 160 GHz). From 120 GHz to 168 GHz, the image rejection is higher than 20dBc and the LO power at RF port is 10 dB lower than the wanted signal.

In order to determine the output power at 1dB compression, the conversion gain versus the input power is shown in Figure 11 below. It was measured for an input signal at 20 MHz and at different LO frequencies. The input power at 1dB of compression is greater than 7 dBm, giving an output power at 1dB of compression between -6 dBm and -3 dBm.

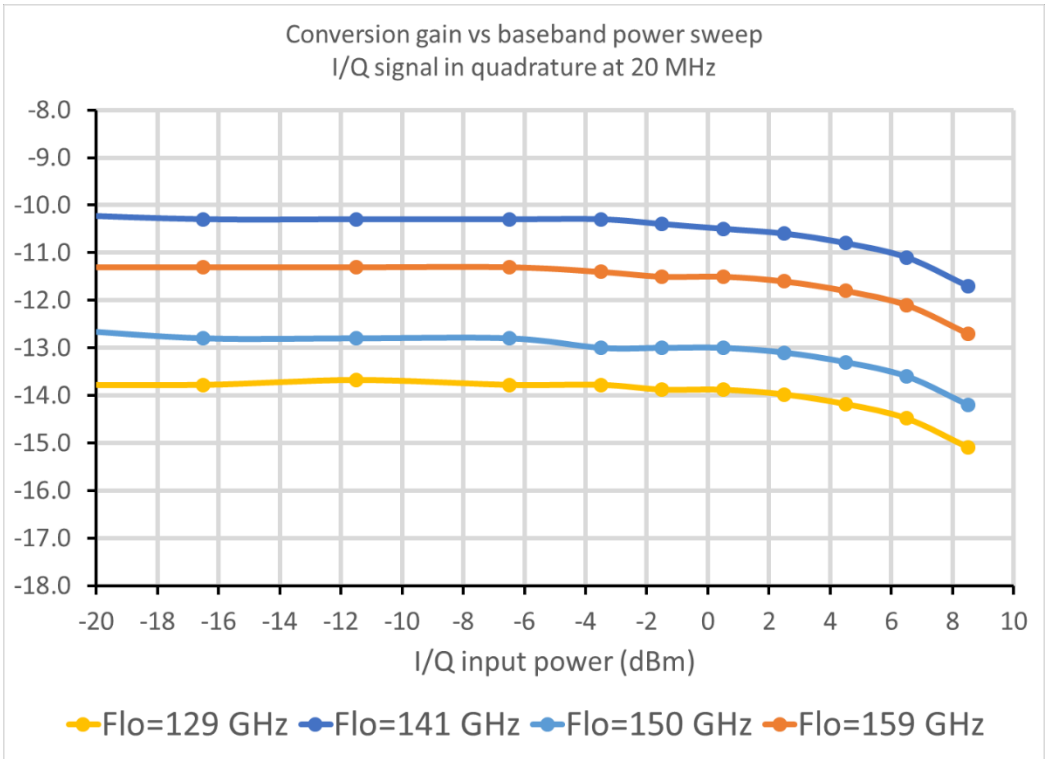

Figure 11 : Measurement results versus baseband Input power at LO power = - 5 dBm.

To measure the conversion gain as a function of the signal frequency (see Figure 12), the 90° hybrid coupler is removed (not wideband enough) to keep only the 180° hybrid coupler which covers the 5 MHz to 1.5 GHz band. As expected, the IF bandwidth is greater than 1.3 GHz that allows a frequency channel up to 2 GHz.

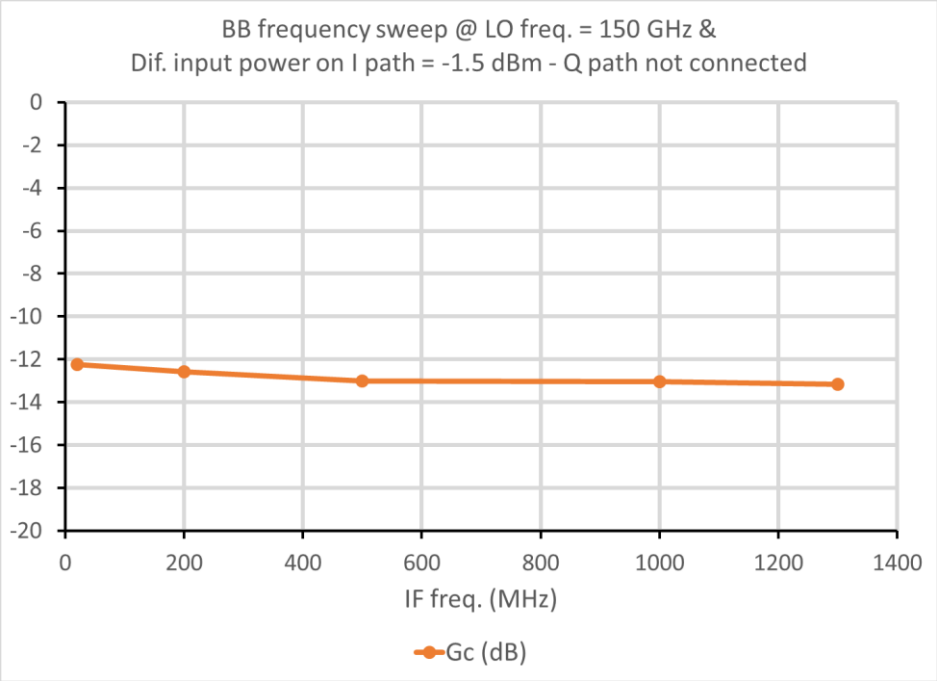

Figure 12 : Measurement results versus frequency of I/Q signals.

A key performance for transmitting a D-band high-level modulation signal is the linearity of the modulator, which is shown in Figure 13. The results are very good, and the 3rd order intermodulation (IM3) is still higher than 30 dBc for an output power of -10 dBm, resulting in an output third-order intercept point (OIP3) higher than -5 dBm. As expected, the IM3 is around 50 dBc (20 dB improvement) for in input power of -5 dBm (10 dB back off).

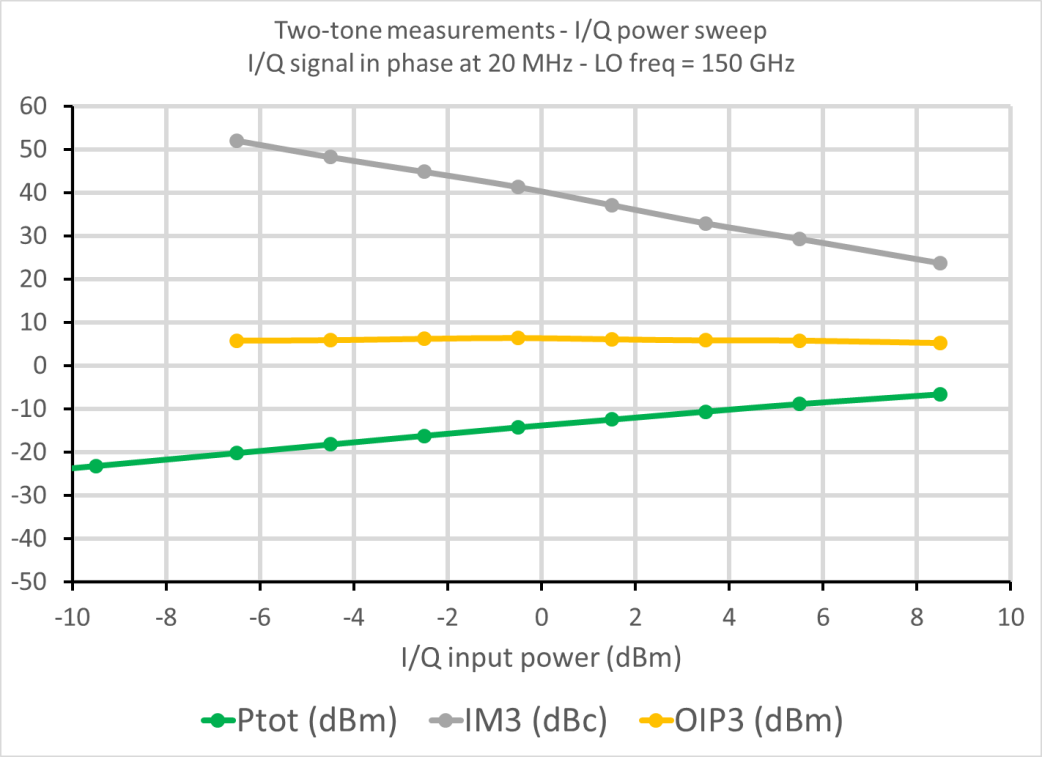

Figure 13 : Two tone measurements versus total power of I/Q signals.

3. Integrated control & monitoring building blocks

3.1 Design description

As it was introduced in D2.1 and according to the latest specifications in D1.5, a SPI interface is selected to control the different chips. In the second tapeout, a first implementation of the integrated SPI slave with test resources was submitted. The goal of this test design is to verify that the registers are written/read correctly when driven from the SPI master and that the interface with the DAC is correct.

A block diagram of the implemented SPI slave is depicted in Figure 14 below. The CLK block is the integrated system clock, which drives the synchronous implementation of the SPI slave. This CLK block was already tested standalone and reported in deliverable D2.2. It has a nominal working frequency of around 70 MHz. A low signal on RESETN input port asynchronously resets the component.

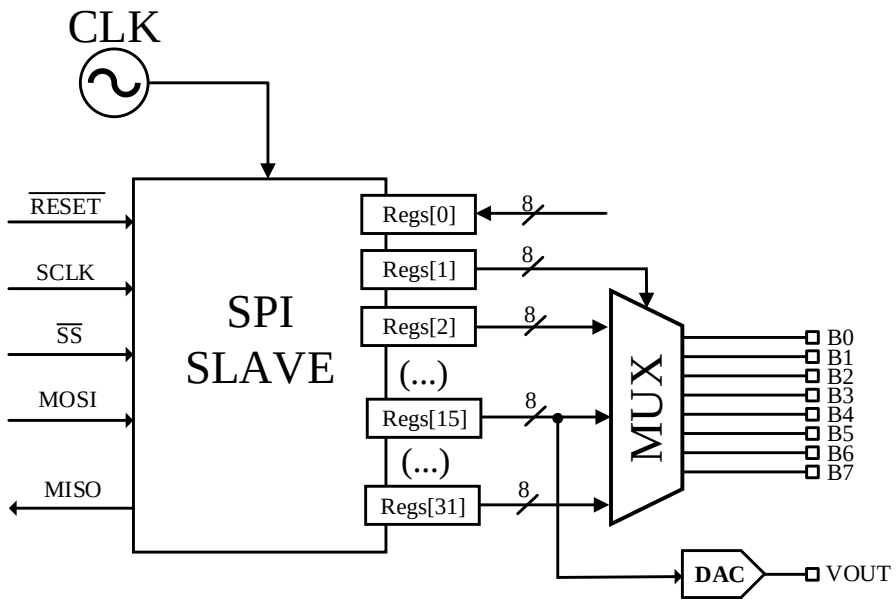

Figure 14: Block diagram of the implemented SPI slave

As observed, the SPI slave block contains a set of 32 8-bit registers. Regs[0] is READ only, while the remaining 31 registers are WRITE registers. In order to test that all the registers work correctly and at the same time require a manageable number of chip pads, a multiplexer structure is implemented, where regs[1] is used to select which register value can be read at the MUX output. The 8-bit MUX output is both routed to the read only regs[0], to read the value from the SPI interface, and to 8 output pads on the chip, so that they can be read directly from outside as well.

The communications between a SPI master and the slave involves the following signals:

- SCK: Master produced clock to synchronize data transfer.
- SS: Slave select.
- MOSI: Master output, slave input.
- MISO: Master input, slave output.
- RSTN: Active low reset.

The master initiates the transaction by pulling the SS wire low. A SCK line, driven by the master, provides a clock signal to synchronize the bits in the data lines. The master transmits data via the MOSI line and receives data via the MISO line.

Each transaction between this SPI slave component and the SPI master consists of an 8-bit command, followed by a 8-bit data transfer. The MSB of the 8-bit command consists of an operating code which specifies the type of operation (read/write). This bit is followed by a 7-bit address. The address determines which register ł the slave writes to (in case of a write operation) or the register from which data has to be read (in case of a read operation). Once the 8-bit command is sent, the data to be written/read is transferred through MOSI/MISO lines.

Command:

MSB							**LSB**
R/W	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

Data:

MSB							**LSB**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

3.2 Test setup

The SPI slave block has been implemented during the second tapeout of the DREAM project, together with other test structures, using the 55-nm BiCMOS process of STMicroelectronics. A photograph of the die is shown in Figure 15. It occupies an area of 0.765 mm x 0.765 mm, limited by the number and size of the pads, while the size of the SPI slave is only 0.1 mm x 0.1 mm.

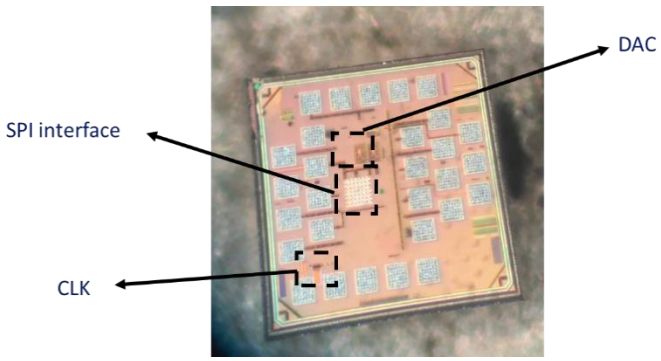

Figure 15: Photograph of the manufactured chip with the control and monitoring blocks

The SPI master that sends the different commands to the slave is implemented in a single-board computer, a BeagleBone Black ®, where a custom software sends the SPI commands and provides a friendly interface to the user. A custom made shield is placed on top of the BeagleBone, which provides signal conditioning and DC supply to the chip. A photograph of the SBC with the shield can be observed in Figure 16.

Figure 16: Photograph of the BeagleBone SBC with the custom shield

The chip is measured using on-wafer probes, which are then connected to the SBC shield. The control software embedded in the SBC is controlled from a laptop, using either ssh and commands in the terminal or graphically using VNC. The DAC output is connected to a multimeter to read the produced output voltage. The same DAC output is connected to a 26.5-GHz Keysight Spectrum Analyzer, using a BNC tee and DC-block, in order to measure the clock spurs on the DAC output. A picture of the described test setup is shown in Figure 17 below.

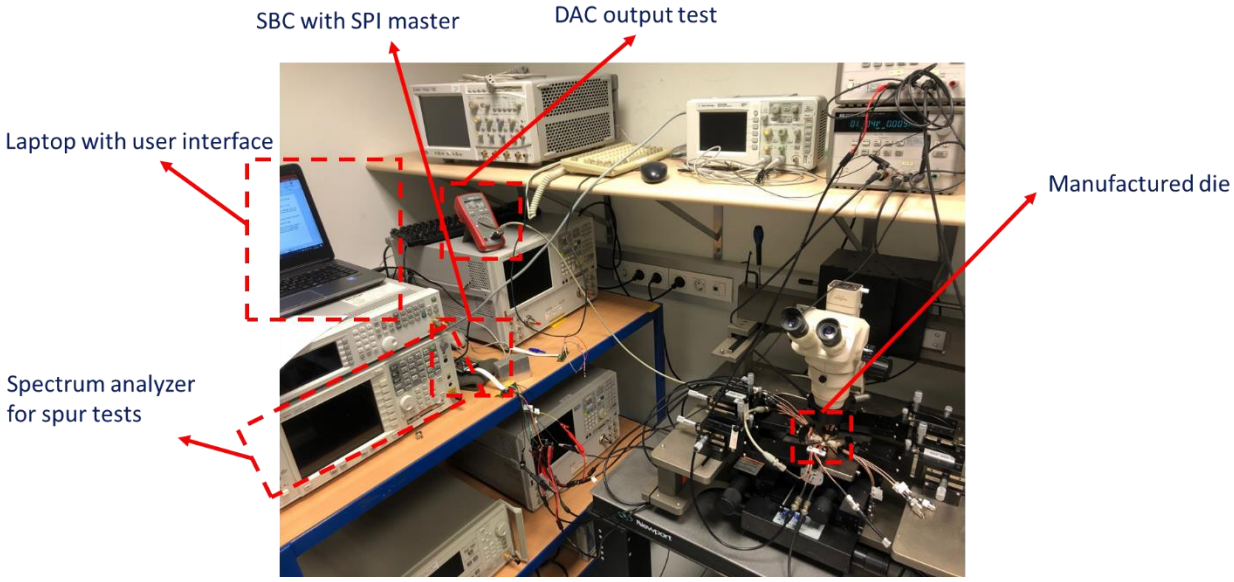

Figure 17: Photograph of the setup to test the control and monitoring blocks

3.3 Test results

To verify the SPI interface, all 0-255 values (0x00 to 0xFF in hexadecimal) have been written to and read from each of the registers, thanks to the multiplexer test structure described in section 15. The read value is shown in the control terminal. Figure 18 shows a snapshot of the control terminal during the test procedure. It has been verified that all values can be written to

and read from all the registers. It has been also verified that the block works with SPI communication speeds in the range between 50 kHz and 2 MHz.

Figure 18: Values read in the SPI interface tests

In this test chip, as a mitigation plan in case the integrated clock did not work as expected, the clock output is not connected directly to the SPI slave inside the chip, but routed to the outside and then introduced again. This way, an external clock can be used if necessary. This causes an extra loading to the clock buffers, bigger than what it can be expected in the final integrated chips. To overcome this extra loading, a Vdd of 1.3V is used to bias the internal clock and its buffers instead of the nominal 1V.

As for the DAC, connected to regs[15], it is tested by sending all 0-255 control words and reading the output voltage in the multimeter. The results are shown in Figure 19. A linear response in the output voltage from 0 to 1.4 V is observed, with a differential non-linearity (DNL) smaller than 0.9 LSB in the worst case. The difference in the measured output voltages is 2.5% in average.

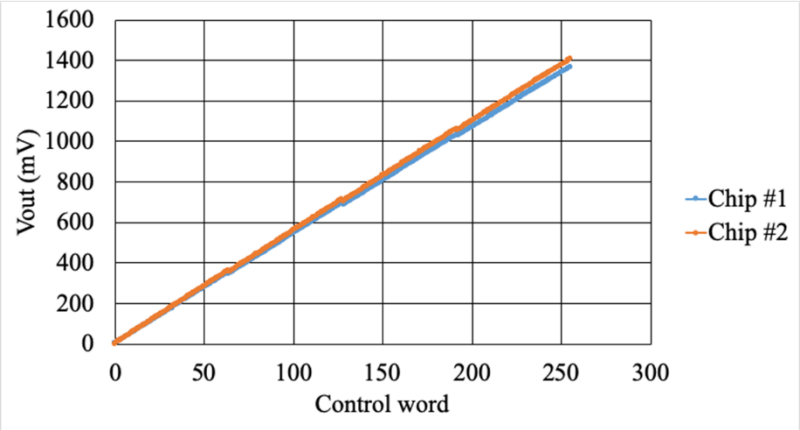

Figure 19: Measured DAC output voltage for 2 different chips.

The spur content in the DAC output signal has also been measured. As it has been said, the SPI slave works with an internal clock of around 70 MHz, which can produce spurs in the DACs used to bias the phased array circuits and consequently affect the quality of the wideband transmitted signal. Figure 20 shows the spur content of the DAC output signal, when measured using a spectrum analyzer – thus, when the load is 50 Ω. It is observed that the biggest spur corresponds to the third harmonic of the fundamental oscillation frequency of the clock. It is difficult to assess at this point the impact that these spurs can have on the real signal transmitted using the final integrated chips. However, as a mitigation plan, the clock can be turned off from the SBC controller using the developed software, and only be turned on during SPI communications. In this case, the output spectrum is clean as shown in Figure 21. It has been verified that turning the system clock on and off has no effect on the registers, as they hold their value. Therefore, it can be used as a safe mitigation plan.

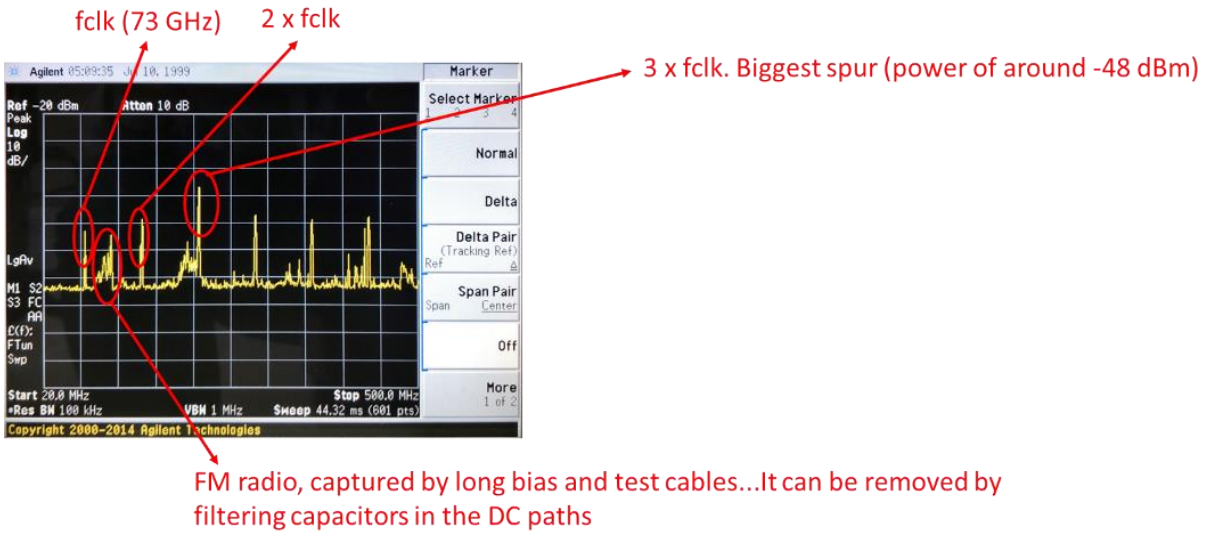

Figure 20: Spur content of the DAC output signal when the CLK is on

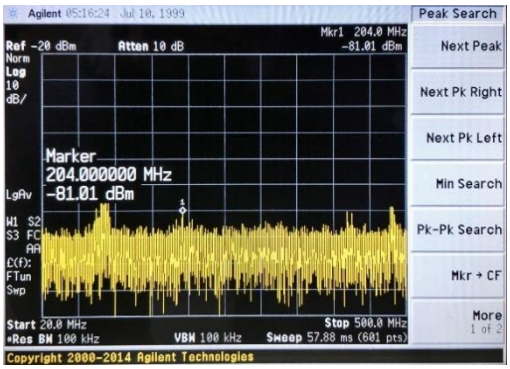

Figure 21: Spur content of the DAC output signal when the CLK is off

4. Conclusions

The final specifications of the I/Q up-conversion block were described in section D1.5 and are compared to the measurement results in Table 1. As shown, most of the specifications are met, except for the conversion gain and the output power at the 1 dB compression point. Both can be easily corrected by boosting the input power by 3 dB and by increasing the gain of the VGA which is in the TX antenna driver chip by 3 dB.

Table 1: Comparison of final specifications (table 5.2 of D1.5) and measurements.

Parameter	Specifications in D1.5	Measurement Results	Comments.
Input Baseband Frequency	1300 MHz	> 1300 MHz	@ 1dB Bandwidth
Input LO frequency	140-160 GHz	140-160 GHz	D-band doubler not included in IQMOD_V2
Required LO drive	> -6 dBm	> -10 dBm	
Output RF Frequency	140-160 GHz	140-160 GHz	
Conversion Gain	-6 (Typ.)	-12 (Typ.)	Including I&Q splitting
Gain ripple in 2-GHz channels	<±0.5 dB	<±0.5 dB	
Output IP3	> 5 dBm	> 5 dBm	
Output Power @1dB comp.	> -3 dBm	> -6 dBm	
Image Rejection Ratio (IRR)	> 15 dB	> 20 dB (typ: 35 dB)	Caused by I/Q imbalance
LO-RF leakage (uncalibrated)	< -10 dBc	< - 8 dBc	with respect to overall signal power when diff. input voltage is 100mVrms at the I&Q branches
Input Return loss @ BB port	> 10 dB	Not measured	
Input Return loss @ RF port	> 10 dB	Not measured	
Input impedance @ BB port	100 Ω, dif.	100 Ω, dif.	DC coupled.
Output impedance @ RF port	50 Ω, single ended	50 Ω, single ended	
Input impedance @ LO port	50 Ω, single ended	50 Ω, single ended	
DC current	< 140 mA	125 mA	Without D-band doubler
Supply Voltage	2.5 Volt	2.5 Volt	

In addition, effort has also been placed in the design of the blocks to control the different circuits in the transceiver, as precise control of the VGAs, LNA, PA and phase shifter is required. An integrated SPI slave has been implemented and completely validated.

References

[1] Paul R. Gray, Paul J. Hurst, Srephen H. Lewis, Robert G. Meyer, "Analysis and Design of analog Integrated Circuits", John Wiley & Sons, Inc, Fourth Edition, 2001.